

# Data Sheet

## S6B1713

65 COM / 132 SEG DRIVER & CONTROLLER FOR STN LCD

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### **Precautions for Light**

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

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## INTRODUCTION

The S6B1713 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 commons and 132 segments driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip Display Data RAM of 65 x 132 bits. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

## FEATURES

### Driver Output Circuits

- 65 common outputs / 132 segment outputs

### On-chip Display Data RAM

- Capacity: 65 x 132 = 8,580 bits

### Applicable Duty Ratios

| Duty ratio | Applicable LCD bias | Maximum display area |
|------------|---------------------|----------------------|
| 1/65       | 1/7 or 1/9          | 65 × 132             |
| 1/49       | 1/6 or 1/8          | 49 × 132             |
| 1/33       | 1/5 or 1/6          | 33 × 132             |

### Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- Serial interface (only write operation) available

### Function Set

- Various instructions sets
- H/W, S/W reset capable

### Built-in Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x2, x3, x4, x5)
- Voltage regulator (temperature coefficient: -0.05%/°C, -0.2%/°C)
- Voltage follower
- Electronic contrast control function (64 steps)

### Operating Voltage Range

- Supply voltage1 (V<sub>DD</sub>): 2.4 to 3.6 V
- Supply voltage2 (V<sub>DD</sub>): 2.4 to 5.5 V (Select by Product code)
- LCD driving voltage (V<sub>LCD</sub> = V<sub>O</sub> - V<sub>SS</sub>): 4.0 to 15.0 V

### Low Power Consumption

- 70 μA Typ. (V<sub>DD</sub> = 3V, x4 boosting, V<sub>O</sub> = 11V, internal power supply ON)
- 10 μA Max. (during power save [standby] mode)

### Package Type

- Gold bumped chip or TCP

## Series Specifications

| Product code    | TEMPS pin            | Temperature coefficient | Package type | Chip thickness | VDD Range  |
|-----------------|----------------------|-------------------------|--------------|----------------|------------|
| S6B1713A01-B0CZ | 0<br>(Vss connected) | -0.05%/°C               | COG          | 670 μm         | 2.4~3.6[V] |
| S6B1713A01-B0CY |                      |                         |              | 470 μm         |            |
| S6B1713A11-B0CZ | 1<br>(VDD connected) | -0.2%/°C                |              | 670 μm         |            |
| S6B1713A11-B0CY |                      |                         |              | 470 μm         |            |
| S6B1713A01-xxX0 | 0<br>(Vss connected) | -0.05%/°C               | TCP          | 670 μm         |            |
| S6B1713A01-xxXN |                      |                         |              | 470 μm         |            |
| S6B1713A11-xxX0 | 1<br>(VDD connected) | -0.2%/°C                |              | 670 μm         |            |
| S6B1713A11-xxXN |                      |                         |              | 470 μm         |            |
| S6B1713A05-B0CZ | 0<br>(Vss connected) | -0.05%/°C               | COG          | 670 μm         | 2.4~5.5[V] |
| S6B1713A05-B0CY |                      |                         |              | 470 μm         |            |
| S6B1713A15-B0CZ | 1<br>(VDD connected) | -0.2%/°C                |              | 670 μm         |            |
| S6B1713A15-B0CY |                      |                         |              | 470 μm         |            |
| S6B1713A05-xxX0 | 0<br>(Vss connected) | -0.05%/°C               | TCP          | 670 μm         |            |
| S6B1713A05-xxXN |                      |                         |              | 470 μm         |            |
| S6B1713A15-xxX0 | 1<br>(VDD connected) | -0.2%/°C                |              | 670 μm         |            |
| S6B1713A15-xxXN |                      |                         |              | 470 μm         |            |

\* xx: TCP ordering number

## BLOCK DIAGRAM

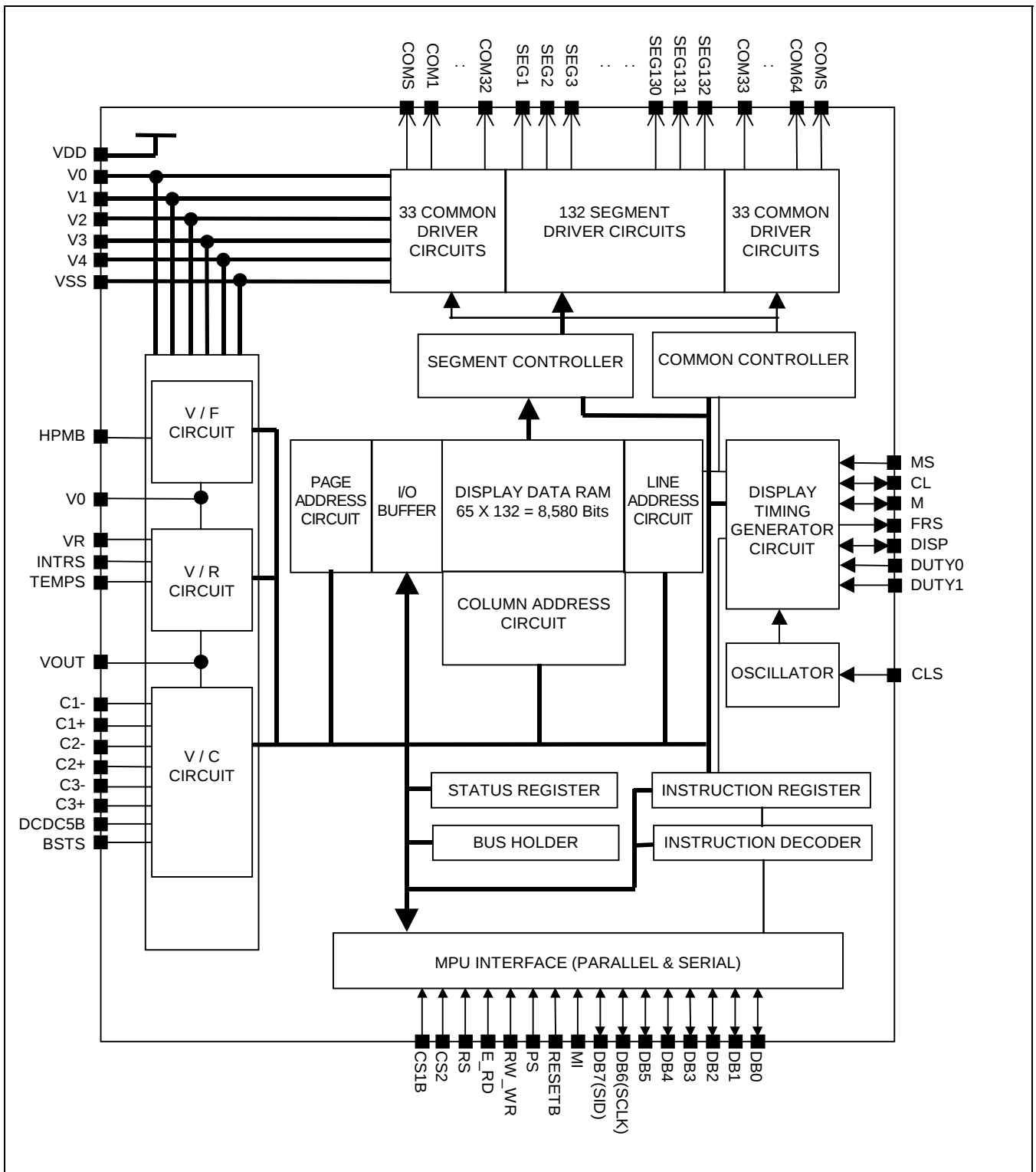


Figure 1. Block Diagram

## PAD CONFIGURATION

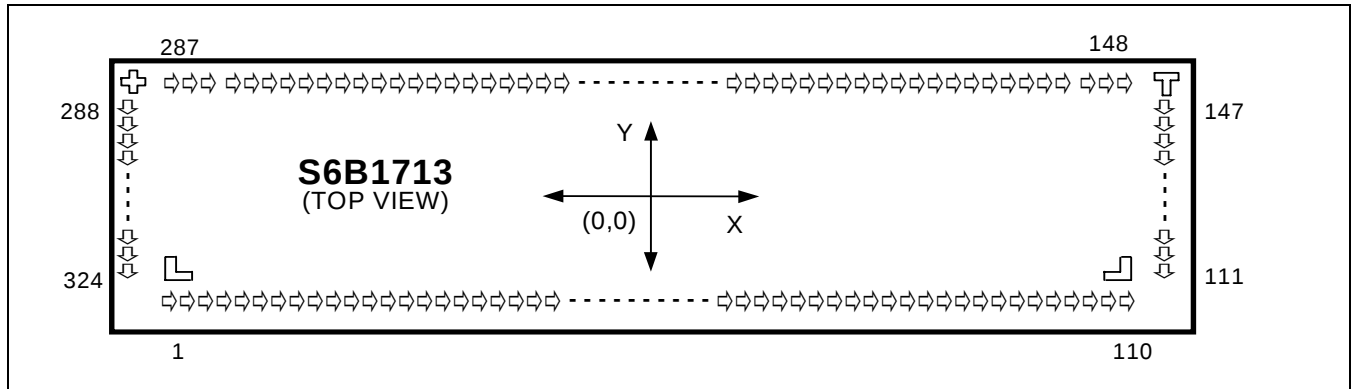


Figure 2. S6B1713 Chip Configuration

Table 1. S6B1713 Pad Dimensions

| Items             | Pad No.    | Size      |      | Unit |
|-------------------|------------|-----------|------|------|
|                   |            | X         | Y    |      |
| Chip size         | -          | 10860     | 2920 | μm   |
| Pad pitch         | 1 to 110   | 90        |      |      |
|                   | 111 to 324 | 70        |      |      |
| Bumped pad size   | 1 to 110   | 56        | 114  |      |
|                   | 111 to 147 | 108       | 50   |      |
|                   | 148 to 287 | 50        | 108  |      |
|                   | 288 to 324 | 108       | 50   |      |
| Bumped pad height | 1 to 324   | 17 (Typ.) |      |      |

Figure 3. COG Align Key Coordinate

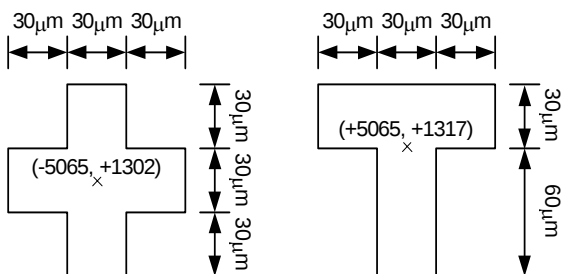
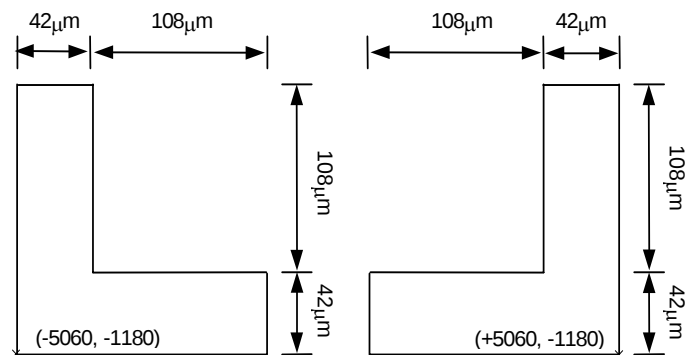


Figure 4. ILB Align Key Coordinate(with Gold Bump \*)



\* When designing electrode pattern must be prohibited on this area (ILB Align Key). If electrode pattern is used for routing over this area, it can be happened pattern-short through gold bump pattern on ILB Align Key.

## PAD Center Coordinates

Table 2. Pad Center Coordinates

[Unit:  $\mu\text{m}$ ]

| No. | Name   | X     | Y     | No. | Name | X    | Y     | No. | Name   | X    | Y     |
|-----|--------|-------|-------|-----|------|------|-------|-----|--------|------|-------|
| 1   | DUMMY  | -4905 | -1336 | 51  | VDD  | -405 | -1336 | 101 | BSTS   | 4095 | -1336 |
| 2   | DUMMY  | -4815 | -1336 | 52  | VDD  | -315 | -1336 | 102 | DCDC5B | 4185 | -1336 |
| 3   | FRS    | -4725 | -1336 | 53  | VDD  | -225 | -1336 | 103 | VDD    | 4275 | -1336 |
| 4   | M      | -4635 | -1336 | 54  | VDD  | -135 | -1336 | 104 | HPM    | 4365 | -1336 |
| 5   | CL     | -4545 | -1336 | 55  | VDD  | -45  | -1336 | 105 | INTRS  | 4455 | -1336 |
| 6   | DISP   | -4455 | -1336 | 56  | VDD  | 45   | -1336 | 106 | VSS    | 4545 | -1336 |
| 7   | VSS    | -4365 | -1336 | 57  | VOUT | 135  | -1336 | 107 | TEMPS  | 4635 | -1336 |
| 8   | CS1B   | -4275 | -1336 | 58  | VOUT | 225  | -1336 | 108 | VDD    | 4725 | -1336 |
| 9   | CS2    | -4185 | -1336 | 59  | VOUT | 315  | -1336 | 109 | DUMMY  | 4815 | -1336 |
| 10  | VDD    | -4095 | -1336 | 60  | VOUT | 405  | -1336 | 110 | DUMMY  | 4905 | -1336 |
| 11  | RESETB | -4005 | -1336 | 61  | C3+  | 495  | -1336 | 111 | DUMMY  | 5271 | -1280 |
| 12  | RS     | -3915 | -1336 | 62  | C3+  | 585  | -1336 | 112 | DUMMY  | 5271 | -1210 |
| 13  | VSS    | -3825 | -1336 | 63  | C3+  | 675  | -1336 | 113 | COMS   | 5271 | -1140 |
| 14  | RW WR  | -3735 | -1336 | 64  | C3+  | 765  | -1336 | 114 | COM1   | 5271 | -1070 |
| 15  | E RD   | -3645 | -1336 | 65  | C3-  | 855  | -1336 | 115 | COM2   | 5271 | -1000 |
| 16  | VDD    | -3555 | -1336 | 66  | C3-  | 945  | -1336 | 116 | COM3   | 5271 | -930  |
| 17  | DB0    | -3465 | -1336 | 67  | C3-  | 1035 | -1336 | 117 | COM4   | 5271 | -860  |
| 18  | DB1    | -3375 | -1336 | 68  | C3-  | 1125 | -1336 | 118 | COM5   | 5271 | -790  |
| 19  | DB2    | -3285 | -1336 | 69  | C1+  | 1215 | -1336 | 119 | COM6   | 5271 | -720  |
| 20  | DB3    | -3195 | -1336 | 70  | C1+  | 1305 | -1336 | 120 | COM7   | 5271 | -650  |
| 21  | DB4    | -3105 | -1336 | 71  | C1+  | 1395 | -1336 | 121 | COM8   | 5271 | -580  |
| 22  | DB5    | -3015 | -1336 | 72  | C1+  | 1485 | -1336 | 122 | COM9   | 5271 | -510  |
| 23  | DB6    | -2925 | -1336 | 73  | C1-  | 1575 | -1336 | 123 | COM10  | 5271 | -440  |
| 24  | DB7    | -2835 | -1336 | 74  | C1-  | 1665 | -1336 | 124 | COM11  | 5271 | -370  |
| 25  | VSS    | -2745 | -1336 | 75  | C1-  | 1755 | -1336 | 125 | COM12  | 5271 | -300  |
| 26  | VDD    | -2655 | -1336 | 76  | C1-  | 1845 | -1336 | 126 | COM13  | 5271 | -230  |
| 27  | VDD    | -2565 | -1336 | 77  | C2+  | 1935 | -1336 | 127 | COM14  | 5271 | -160  |
| 28  | VDD    | -2475 | -1336 | 78  | C2+  | 2025 | -1336 | 128 | COM15  | 5271 | -90   |
| 29  | DUTY0  | -2385 | -1336 | 79  | C2+  | 2115 | -1336 | 129 | COM16  | 5271 | -20   |
| 30  | DUTY1  | -2295 | -1336 | 80  | C2+  | 2205 | -1336 | 130 | COM17  | 5271 | 50    |
| 31  | VSS    | -2205 | -1336 | 81  | C2-  | 2295 | -1336 | 131 | COM18  | 5271 | 120   |
| 32  | MS     | -2115 | -1336 | 82  | C2-  | 2385 | -1336 | 132 | COM19  | 5271 | 190   |
| 33  | CLS    | -2025 | -1336 | 83  | C2-  | 2475 | -1336 | 133 | COM20  | 5271 | 260   |
| 34  | VDD    | -1935 | -1336 | 84  | C2-  | 2565 | -1336 | 134 | COM21  | 5271 | 330   |
| 35  | MI     | -1845 | -1336 | 85  | VSS  | 2655 | -1336 | 135 | COM22  | 5271 | 400   |
| 36  | PS     | -1755 | -1336 | 86  | VSS  | 2745 | -1336 | 136 | COM23  | 5271 | 470   |
| 37  | VSS    | -1665 | -1336 | 87  | VR   | 2835 | -1336 | 137 | COM24  | 5271 | 540   |
| 38  | VSS    | -1575 | -1336 | 88  | VR   | 2925 | -1336 | 138 | COM25  | 5271 | 610   |
| 39  | VSS    | -1485 | -1336 | 89  | V0   | 3015 | -1336 | 139 | COM26  | 5271 | 680   |
| 40  | VSS    | -1395 | -1336 | 90  | V0   | 3105 | -1336 | 140 | COM27  | 5271 | 750   |
| 41  | VSS    | -1305 | -1336 | 91  | V1   | 3195 | -1336 | 141 | COM28  | 5271 | 820   |
| 42  | VSS    | -1215 | -1336 | 92  | V1   | 3285 | -1336 | 142 | COM29  | 5271 | 890   |
| 43  | VSS    | -1125 | -1336 | 93  | V2   | 3375 | -1336 | 143 | COM30  | 5271 | 960   |
| 44  | VSS    | -1035 | -1336 | 94  | V2   | 3465 | -1336 | 144 | COM31  | 5271 | 1030  |
| 45  | VSS    | -945  | -1336 | 95  | V3   | 3555 | -1336 | 145 | COM32  | 5271 | 1100  |
| 46  | VSS    | -855  | -1336 | 96  | V3   | 3645 | -1336 | 146 | DUMMY  | 5271 | 1170  |
| 47  | VDD    | -765  | -1336 | 97  | V4   | 3735 | -1336 | 147 | DUMMY  | 5271 | 1240  |
| 48  | VDD    | -675  | -1336 | 98  | V4   | 3825 | -1336 | 148 | DUMMY  | 4865 | 1301  |
| 49  | VDD    | -585  | -1336 | 99  | VSS  | 3915 | -1336 | 149 | DUMMY  | 4795 | 1301  |
| 50  | VDD    | -495  | -1336 | 100 | VSS  | 4005 | -1336 | 150 | DUMMY  | 4725 | 1301  |

Table 2. Pad Center Coordinates (Continued)

[Unit:  $\mu\text{m}$ ]

| No. | Name  | X    | Y    | No. | Name  | X     | Y    | No. | Name   | X     | Y    |
|-----|-------|------|------|-----|-------|-------|------|-----|--------|-------|------|
| 151 | DUMMY | 4655 | 1301 | 201 | SEG50 | 1155  | 1301 | 251 | SEG100 | -2345 | 1301 |
| 152 | SEG1  | 4585 | 1301 | 202 | SEG51 | 1085  | 1301 | 252 | SEG101 | -2415 | 1301 |
| 153 | SEG2  | 4515 | 1301 | 203 | SEG52 | 1015  | 1301 | 253 | SEG102 | -2485 | 1301 |
| 154 | SEG3  | 4445 | 1301 | 204 | SEG53 | 945   | 1301 | 254 | SEG103 | -2555 | 1301 |
| 155 | SEG4  | 4375 | 1301 | 205 | SEG54 | 875   | 1301 | 255 | SEG104 | -2625 | 1301 |
| 156 | SEG5  | 4305 | 1301 | 206 | SEG55 | 805   | 1301 | 256 | SEG105 | -2695 | 1301 |
| 157 | SEG6  | 4235 | 1301 | 207 | SEG56 | 735   | 1301 | 257 | SEG106 | -2765 | 1301 |
| 158 | SEG7  | 4165 | 1301 | 208 | SEG57 | 665   | 1301 | 258 | SEG107 | -2835 | 1301 |
| 159 | SEG8  | 4095 | 1301 | 209 | SEG58 | 595   | 1301 | 259 | SEG108 | -2905 | 1301 |
| 160 | SEG9  | 4025 | 1301 | 210 | SEG59 | 525   | 1301 | 260 | SEG109 | -2975 | 1301 |
| 161 | SEG10 | 3955 | 1301 | 211 | SEG60 | 455   | 1301 | 261 | SEG110 | -3045 | 1301 |
| 162 | SEG11 | 3885 | 1301 | 212 | SEG61 | 385   | 1301 | 262 | SEG111 | -3115 | 1301 |
| 163 | SEG12 | 3815 | 1301 | 213 | SEG62 | 315   | 1301 | 263 | SEG112 | -3185 | 1301 |
| 164 | SEG13 | 3745 | 1301 | 214 | SEG63 | 245   | 1301 | 264 | SEG113 | -3255 | 1301 |
| 165 | SEG14 | 3675 | 1301 | 215 | SEG64 | 175   | 1301 | 265 | SEG114 | -3325 | 1301 |
| 166 | SEG15 | 3605 | 1301 | 216 | SEG65 | 105   | 1301 | 266 | SEG115 | -3395 | 1301 |
| 167 | SEG16 | 3535 | 1301 | 217 | SEG66 | 35    | 1301 | 267 | SEG116 | -3465 | 1301 |
| 168 | SEG17 | 3465 | 1301 | 218 | SEG67 | -35   | 1301 | 268 | SEG117 | -3535 | 1301 |
| 169 | SEG18 | 3395 | 1301 | 219 | SEG68 | -105  | 1301 | 269 | SEG118 | -3605 | 1301 |
| 170 | SEG19 | 3325 | 1301 | 220 | SEG69 | -175  | 1301 | 270 | SEG119 | -3675 | 1301 |
| 171 | SEG20 | 3255 | 1301 | 221 | SEG70 | -245  | 1301 | 271 | SEG120 | -3745 | 1301 |
| 172 | SEG21 | 3185 | 1301 | 222 | SEG71 | -315  | 1301 | 272 | SEG121 | -3815 | 1301 |
| 173 | SEG22 | 3115 | 1301 | 223 | SEG72 | -385  | 1301 | 273 | SEG122 | -3885 | 1301 |
| 174 | SEG23 | 3045 | 1301 | 224 | SEG73 | -455  | 1301 | 274 | SEG123 | -3955 | 1301 |
| 175 | SEG24 | 2975 | 1301 | 225 | SEG74 | -525  | 1301 | 275 | SEG124 | -4025 | 1301 |
| 176 | SEG25 | 2905 | 1301 | 226 | SEG75 | -595  | 1301 | 276 | SEG125 | -4095 | 1301 |
| 177 | SEG26 | 2835 | 1301 | 227 | SEG76 | -665  | 1301 | 277 | SEG126 | -4165 | 1301 |
| 178 | SEG27 | 2765 | 1301 | 228 | SEG77 | -735  | 1301 | 278 | SEG127 | -4235 | 1301 |
| 179 | SEG28 | 2695 | 1301 | 229 | SEG78 | -805  | 1301 | 279 | SEG128 | -4305 | 1301 |
| 180 | SEG29 | 2625 | 1301 | 230 | SEG79 | -875  | 1301 | 280 | SEG129 | -4375 | 1301 |
| 181 | SEG30 | 2555 | 1301 | 231 | SEG80 | -945  | 1301 | 281 | SEG130 | -4445 | 1301 |
| 182 | SEG31 | 2485 | 1301 | 232 | SEG81 | -1015 | 1301 | 282 | SEG131 | -4515 | 1301 |
| 183 | SEG32 | 2415 | 1301 | 233 | SEG82 | -1085 | 1301 | 283 | SEG132 | -4585 | 1301 |
| 184 | SEG33 | 2345 | 1301 | 234 | SEG83 | -1155 | 1301 | 284 | DUMMY  | -4655 | 1301 |
| 185 | SEG34 | 2275 | 1301 | 235 | SEG84 | -1225 | 1301 | 285 | DUMMY  | -4725 | 1301 |
| 186 | SEG35 | 2205 | 1301 | 236 | SEG85 | -1295 | 1301 | 286 | DUMMY  | -4795 | 1301 |
| 187 | SEG36 | 2135 | 1301 | 237 | SEG86 | -1365 | 1301 | 287 | DUMMY  | -4865 | 1301 |
| 188 | SEG37 | 2065 | 1301 | 238 | SEG87 | -1435 | 1301 | 288 | DUMMY  | -5271 | 1240 |
| 189 | SEG38 | 1995 | 1301 | 239 | SEG88 | -1505 | 1301 | 289 | DUMMY  | -5271 | 1170 |
| 190 | SEG39 | 1925 | 1301 | 240 | SEG89 | -1575 | 1301 | 290 | COM5   | -5271 | 1100 |
| 191 | SEG40 | 1855 | 1301 | 241 | SEG90 | -1645 | 1301 | 291 | COM64  | -5271 | 1030 |
| 192 | SEG41 | 1785 | 1301 | 242 | SEG91 | -1715 | 1301 | 292 | COM63  | -5271 | 960  |
| 193 | SEG42 | 1715 | 1301 | 243 | SEG92 | -1785 | 1301 | 293 | COM62  | -5271 | 890  |
| 194 | SEG43 | 1645 | 1301 | 244 | SEG93 | -1855 | 1301 | 294 | COM61  | -5271 | 820  |
| 195 | SEG44 | 1575 | 1301 | 245 | SEG94 | -1925 | 1301 | 295 | COM60  | -5271 | 750  |
| 196 | SEG45 | 1505 | 1301 | 246 | SEG95 | -1995 | 1301 | 296 | COM59  | -5271 | 680  |
| 197 | SEG46 | 1435 | 1301 | 247 | SEG96 | -2065 | 1301 | 297 | COM58  | -5271 | 610  |
| 198 | SEG47 | 1365 | 1301 | 248 | SEG97 | -2135 | 1301 | 298 | COM57  | -5271 | 540  |
| 199 | SEG48 | 1295 | 1301 | 249 | SEG98 | -2205 | 1301 | 299 | COM56  | -5271 | 470  |
| 200 | SEG49 | 1225 | 1301 | 250 | SEG99 | -2275 | 1301 | 300 | COM55  | -5271 | 400  |

**Table 2. Pad Center Coordinates (Continued)**

[Unit:  $\mu\text{m}$ ][illegible]

## PIN DESCRIPTION

### POWER SUPPLY

**Table 3. Power Supply Pin Description**

| Name                       | I/O    | Description                                                                                                                                                                                                                                                                                                                                                                  |            |            |            |            |
|----------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|------------|------------|
| VDD                        | Supply | Power supply                                                                                                                                                                                                                                                                                                                                                                 |            |            |            |            |
| VSS                        | Supply | Ground                                                                                                                                                                                                                                                                                                                                                                       |            |            |            |            |
| V0<br>V1<br>V2<br>V3<br>V4 | I/O    | LCD driver supply voltages<br>The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.<br>Voltages should have the following relationship;<br>$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$<br>When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias. |            |            |            |            |
|                            |        | LCD bias                                                                                                                                                                                                                                                                                                                                                                     | V1         | V2         | V3         | V4         |
|                            |        | 1/9 bias                                                                                                                                                                                                                                                                                                                                                                     | (8/9) x V0 | (7/9) x V0 | (2/9) x V0 | (1/9) x V0 |
|                            |        | 1/8 bias                                                                                                                                                                                                                                                                                                                                                                     | (7/8) x V0 | (6/8) x V0 | (2/8) x V0 | (1/8) x V0 |
|                            |        | 1/7 bias                                                                                                                                                                                                                                                                                                                                                                     | (6/7) x V0 | (5/7) x V0 | (2/7) x V0 | (1/7) x V0 |
|                            |        | 1/6 bias                                                                                                                                                                                                                                                                                                                                                                     | (5/6) x V0 | (4/6) x V0 | (2/6) x V0 | (1/6) x V0 |
|                            |        | 1/5 bias                                                                                                                                                                                                                                                                                                                                                                     | (4/5) x V0 | (3/5) x V0 | (2/5) x V0 | (1/5) x V0 |

### LCD DRIVER SUPPLY

**Table 4. LCD Driver Supply Pin Description**

| Name   | I/O | Description                                                                                                                                  |
|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|
| C1-    | O   | Capacitor 1 negative connection pin for voltage converter                                                                                    |
| C1+    | O   | Capacitor 1 positive connection pin for voltage converter                                                                                    |
| C2-    | O   | Capacitor 2 negative connection pin for voltage converter                                                                                    |
| C2+    | O   | Capacitor 2 positive connection pin for voltage converter                                                                                    |
| C3-    | O   | Capacitor 3 negative connection pin for voltage converter                                                                                    |
| C3+    | O   | Capacitor 3 positive connection pin for voltage converter                                                                                    |
| VOU    | I/O | Voltage converter input / output pin                                                                                                         |
| DCDC5B | I   | 5 times boosting circuit enable input pin<br>When this pin is low in 4 times boosting circuit, the 5-times boosting voltage appears at VOUT. |
| VR     | I   | V0 voltage adjustment pin<br>It is valid only when on-chip resistors are not used (INTRS = "L").                                             |

## SYSTEM CONTROL

Table 5. System Control Pin Description

| Name  | I/O | Description                                                                                                                                                                                                                                                         |     |             |                      |        |        |        |        |
|-------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------|----------------------|--------|--------|--------|--------|
| MS    | I   | This is the test pin.<br>MS pin should be fixed "H", not "L".                                                                                                                                                                                                       |     |             |                      |        |        |        |        |
|       |     | MS                                                                                                                                                                                                                                                                  | CLS | OSC circuit | Power supply circuit | CL     | M      | FRS    | DISP   |
|       |     | H                                                                                                                                                                                                                                                                   | H   | Enabled     | Enabled              | Output | Output | Output | Output |
|       |     |                                                                                                                                                                                                                                                                     | L   | Disable     | Enabled              | Input  | Output | Output | Output |
| CLS   | I   | Built-in oscillator circuit enable / disable select pin<br>– CLS = "H": enable<br>– CLS = "L": disable (external display clock input to CL pin)                                                                                                                     |     |             |                      |        |        |        |        |
| CL    | O   | This pin is for monitoring the display clock output<br>The CL pin must be opened.                                                                                                                                                                                   |     |             |                      |        |        |        |        |
| M     | O   | This pin is for monitoring the LCD AC signal output.<br>The M pin must be opened.                                                                                                                                                                                   |     |             |                      |        |        |        |        |
| FRS   | O   | Static driver segment output pin<br>This pin is used together with the M pin.                                                                                                                                                                                       |     |             |                      |        |        |        |        |
| DISP  | O   | This pin is for monitoring the LCD display blanking control output<br>The DISP pin must be opened.                                                                                                                                                                  |     |             |                      |        |        |        |        |
| INTRS | I   | Internal resistors select pin<br>This pin selects the resistors for adjusting V0 voltage level.<br>– INTRS = "H": use the internal resistors.<br>– INTRS = "L": use the external resistors.<br>V0 voltage is controlled with VR pin and external resistive divider. |     |             |                      |        |        |        |        |
| HPM   | I   | Power control pin of the power supply circuit for LCD driver<br>– HPM = "H": high power mode<br>– HPM = "L": normal mode                                                                                                                                            |     |             |                      |        |        |        |        |
| TEMPS | I   | Selects temperature coefficient of the reference voltage<br>– TEMPS = "L": -0.05%/°C<br>– TEMPS = "H": -0.2%/°C                                                                                                                                                     |     |             |                      |        |        |        |        |

Table 5. System Control Pin Description (Continued)

| Name           | I/O | Description                                                                                                                         |                                 |                              |
|----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------------------------------|
| BSTS           | I   | Selects input voltages of the built-in voltage converter                                                                            |                                 |                              |
|                |     | BSTS                                                                                                                                | Voltage converter input voltage | Remarks                      |
|                |     | L                                                                                                                                   | 4V                              | $V_{DD} > 4V$                |
|                |     | H                                                                                                                                   | $V_{DD}$                        | $2.4V \leq V_{DD} \leq 5.5V$ |
|                |     | NOTE: Because the maximum voltage of $V_{DD}$ has been changed to 5.5V, we strongly recommend that BSTS pin should be fixed to "H". |                                 |                              |
| DUTY0<br>DUTY1 | I   | The LCD driver duty ratio depends on the following table                                                                            |                                 |                              |
|                |     | DUTY1                                                                                                                               | DUTY0                           | Duty ratio                   |
|                |     | L                                                                                                                                   | L                               | 1/33                         |
|                |     | L                                                                                                                                   | H                               | 1/49                         |
|                |     | H                                                                                                                                   | L/H                             | 1/65                         |

## MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

| Name        | I/O | Description                                                                                                                                                             |                |             |                                                                                                          |            |               |              |
|-------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-------------|----------------------------------------------------------------------------------------------------------|------------|---------------|--------------|
| RESETB      | I   | Reset input pin<br>When RESETB is “L”, initialization is executed.                                                                                                      |                |             |                                                                                                          |            |               |              |
| PS          | I   | Parallel / Serial data input select input                                                                                                                               |                |             |                                                                                                          |            |               |              |
|             |     | PS                                                                                                                                                                      | Interface mode | Chip select | Data / instruction                                                                                       | Data       | Read / Write  | Serial clock |
|             |     | H                                                                                                                                                                       | Parallel       | CS1B, CS2   | RS                                                                                                       | DB0 to DB7 | E_RD<br>RW_WR | -            |
|             |     | L                                                                                                                                                                       | Serial         | CS1B, CS2   | RS                                                                                                       | SID(DB7)   | Write only    | SCLK(DB6)    |
|             |     | *NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR, MI must be fixed to either “H” or “L”. |                |             |                                                                                                          |            |               |              |
| MI          | I   | Microprocessor interface selects input pin<br>– MI = "H": 6800-series MPU interface<br>– MI = "L": 8080-series MPU interface                                            |                |             |                                                                                                          |            |               |              |
| CS1B<br>CS2 | I   | Chip select input pins<br>Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”.<br>When chip select is non-active, DB0 to DB7 may be high impedance.  |                |             |                                                                                                          |            |               |              |
| RS          | I   | Register select input pin<br>– RS = "H": DB0 to DB7 are display data<br>– RS = "L": DB0 to DB7 are control data                                                         |                |             |                                                                                                          |            |               |              |
| RW_WR       | I   | Read / Write execution control pin                                                                                                                                      |                |             |                                                                                                          |            |               |              |
|             |     | MI                                                                                                                                                                      | MPU type       | RW_WR       | Description                                                                                              |            |               |              |
|             |     | H                                                                                                                                                                       | 6800-series    | RW          | Read / Write control input pin<br>– RW = “H”: read<br>– RW = “L”: write                                  |            |               |              |
|             |     | L                                                                                                                                                                       | 8080-series    | /WR         | Write enable clock input pin<br>The data ON DB0 to DB7 are latched at the rising edge of the /WR signal. |            |               |              |

Table 6. Microprocessor Interface Pin Description (Continued)

| Name       | I/O | Description                                                                                                                                                                                                                                                                                                              |             |      |                                                                                                                                                                                         |
|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E_RD       | I   | Read / Write execution control pin                                                                                                                                                                                                                                                                                       |             |      |                                                                                                                                                                                         |
|            |     | MI                                                                                                                                                                                                                                                                                                                       | MPU type    | E_RD | Description                                                                                                                                                                             |
|            |     | H                                                                                                                                                                                                                                                                                                                        | 6800-series | E    | Read / Write control input pin<br>– RW = "H": When E is "H", DB0 to DB7 are in an output status.<br>– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal. |
|            |     | L                                                                                                                                                                                                                                                                                                                        | 8080-series | /RD  | Read enable clock input pin<br>When /RD is "L", DB0 to DB7 are in an output status.                                                                                                     |
|            |     |                                                                                                                                                                                                                                                                                                                          |             |      |                                                                                                                                                                                         |
| DB0 to DB7 | I/O | 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");<br>– DB0 to DB5: high impedance<br>– DB6: serial input clock (SCLK)<br>– DB7: serial input data (SID)<br>When chip select is not active, DB0 to DB7 may be high impedance. |             |      |                                                                                                                                                                                         |

## LCD DRIVER OUTPUTS

Table 7. LCD Driver Outputs Pin Description

| Name                 | I/O | Description                                                                                                            |   |                               |                 |
|----------------------|-----|------------------------------------------------------------------------------------------------------------------------|---|-------------------------------|-----------------|
| SEG1<br>to<br>SEG132 | O   | LCD segment driver outputs<br>The display data and the M signal control the output voltage of segment driver.          |   |                               |                 |
|                      |     | Display data                                                                                                           | M | Segment driver output voltage |                 |
|                      |     |                                                                                                                        |   | Normal display                | Reverse display |
|                      |     | H                                                                                                                      | H | V0                            | V2              |
|                      |     | H                                                                                                                      | L | Vss                           | V3              |
|                      |     | L                                                                                                                      | H | V2                            | V0              |
|                      |     | L                                                                                                                      | L | V3                            | Vss             |
|                      |     | Power save mode                                                                                                        |   | Vss                           | Vss             |
|                      |     |                                                                                                                        |   |                               |                 |
| COM1<br>to<br>COM64  | O   | LCD common driver outputs<br>The internal scanning data and M signal control the output voltage of common driver.      |   |                               |                 |
|                      |     | Scan data                                                                                                              | M | Common driver output voltage  |                 |
|                      |     | H                                                                                                                      | H | Vss                           |                 |
|                      |     | H                                                                                                                      | L | V0                            |                 |
|                      |     | L                                                                                                                      | H | V1                            |                 |
|                      |     | L                                                                                                                      | L | V4                            |                 |
|                      |     | Power save mode                                                                                                        |   | Vss                           |                 |
|                      |     |                                                                                                                        |   |                               |                 |
| COMS                 | O   | Common output for the icons<br>The output signals of two pins are same. When not used, these pins should be left open. |   |                               |                 |

NOTE: DUMMY - These pins should be opened (floated).

## FUNCTIONAL DESCRIPTION

### MICROPROCESSOR INTERFACE

#### Chip Select Input

There are CS1B and CS2 pins for Chip Selection. The S6B1713 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E\_RD, and RW\_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

#### Parallel / Serial Interface

S6B1713 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

**Table 8. Parallel / Serial Interface Mode**

| PS | Type     | CS1B | CS2 | MI | Interface mode       |
|----|----------|------|-----|----|----------------------|
| H  | Parallel | CS1B | CS2 | H  | 6800-series MPU mode |
|    |          |      |     | L  | 8080-series MPU mode |
| L  | Serial   | CS1B | CS2 | *  | Serial-mode          |

\* : Don't care

#### Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by MI as shown in table 9. The type of data transfer is determined by signals at RS, E\_RD and RW\_WR as shown in table10.

**Table 9. Microprocessor Selection for Parallel Interface**

| MI | CS1B | CS2 | RS | E_RD | RW_WR | DB0 to DB7 | MPU bus     |
|----|------|-----|----|------|-------|------------|-------------|
| H  | CS1B | CS2 | RS | E    | RW    | DB0 to DB7 | 6800-series |
| L  | CS1B | CS2 | RS | /RD  | /WR   | DB0 to DB7 | 8080-series |

**Table 10. Parallel Data Transfer**

| Common | 6800-series |            | 8080-series |             | Description                               |
|--------|-------------|------------|-------------|-------------|-------------------------------------------|
| RS     | E_RD (E)    | RW_WR (RW) | E_RD (/RD)  | RW_WR (/WR) |                                           |
| H      | H           | H          | L           | H           | Display data read out                     |
| H      | H           | L          | H           | L           | Display data write                        |
| L      | H           | H          | L           | H           | Register status read                      |
| L      | H           | L          | H           | L           | Writes to internal register (instruction) |

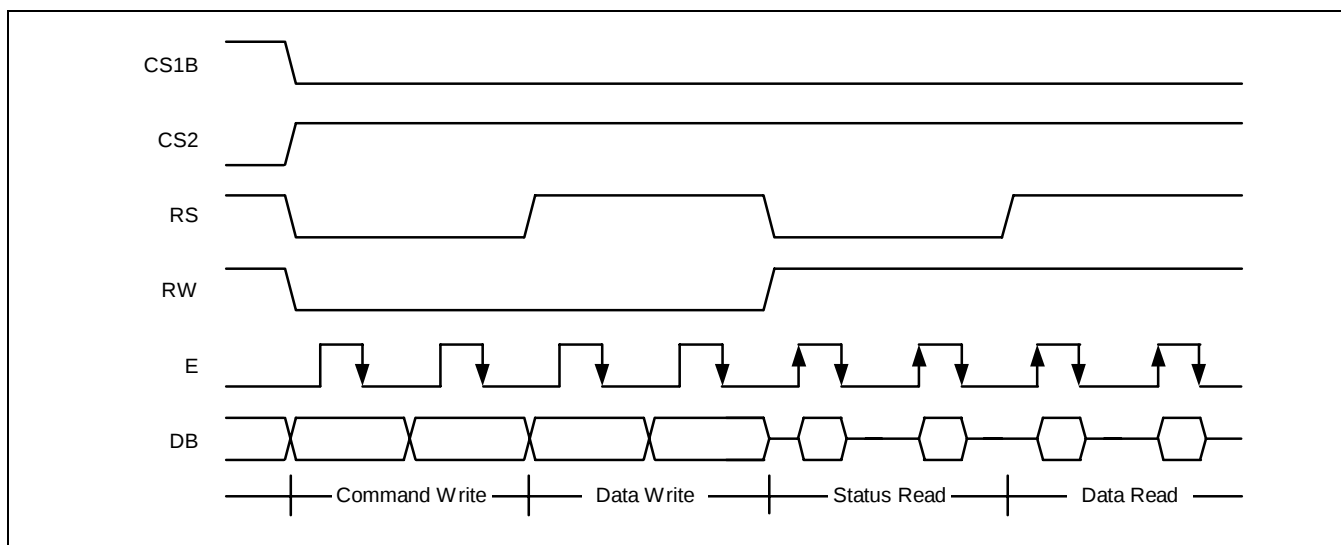


Figure 5. 6800-Series MPU Interface protocol (PS="H", MI="H")

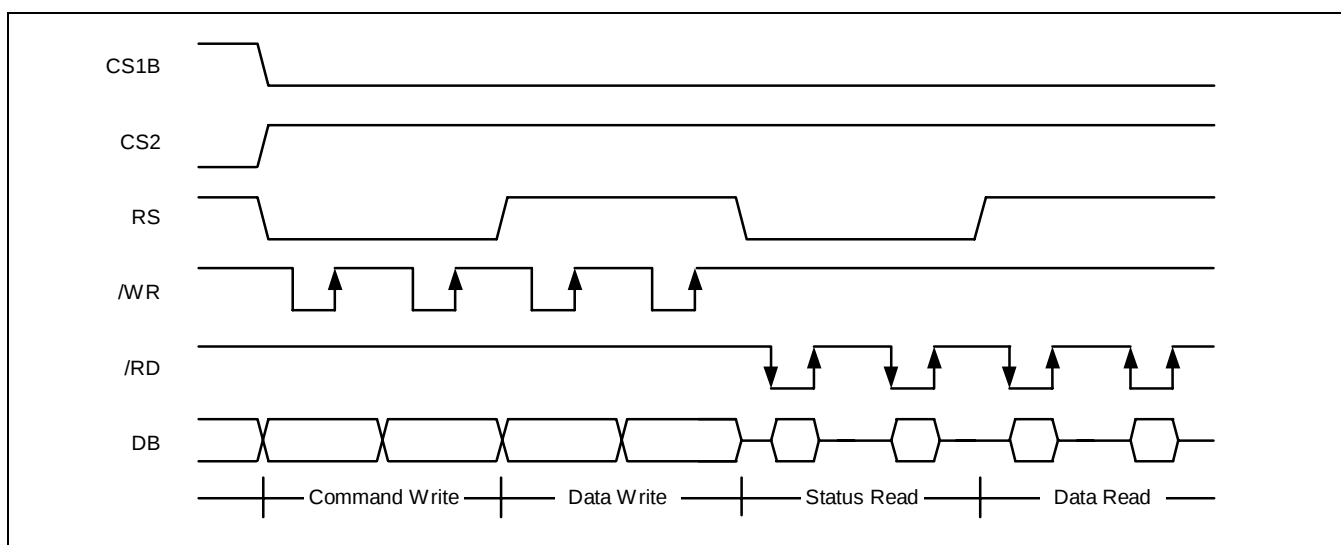


Figure 6. 8080-Series MPU Interface Protocol (PS="H", MI="L")

### Serial Interface (PS = "L", MI="H" or "L")

When the S6B1713 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

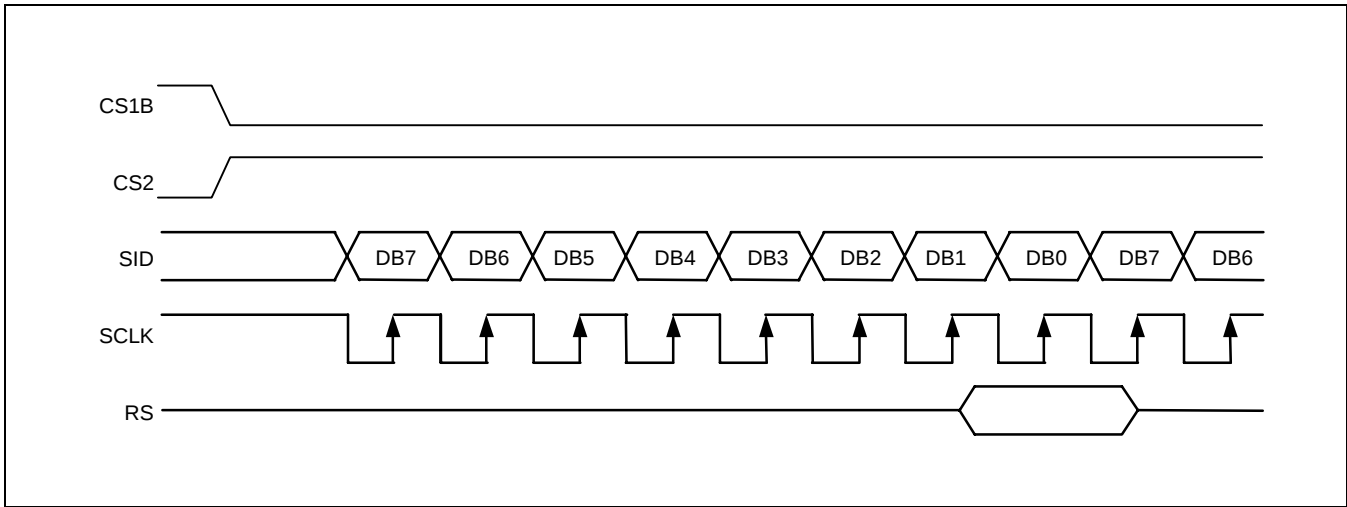


Figure 7. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B1713 is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B1713 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

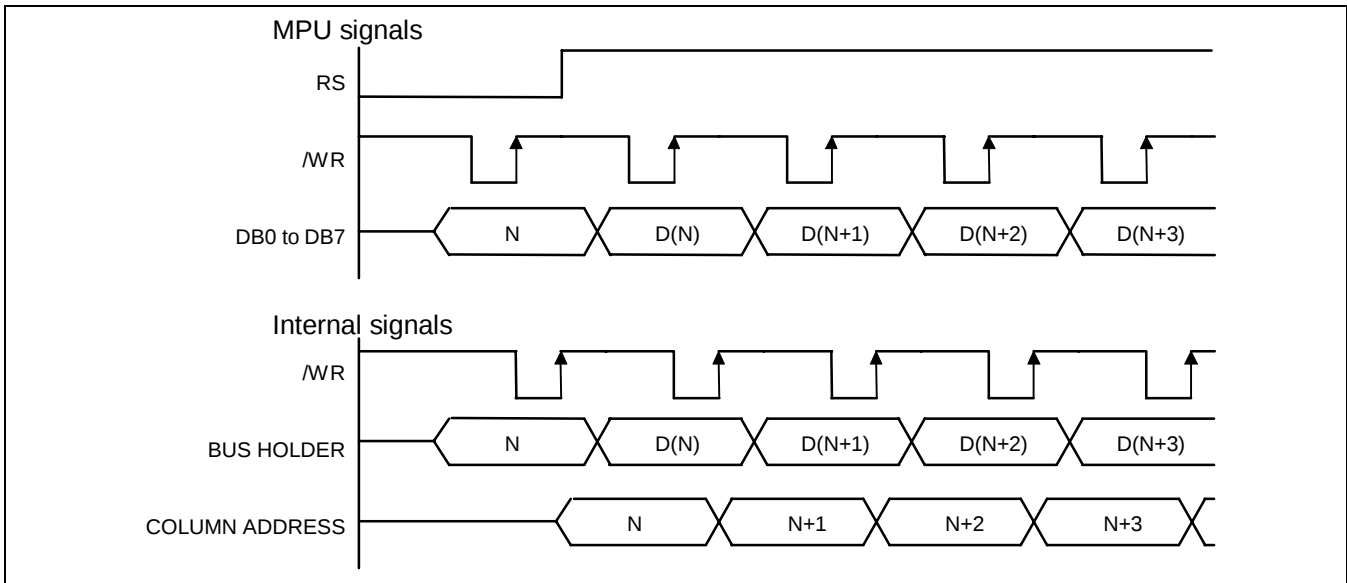


Figure 8. Write Timing

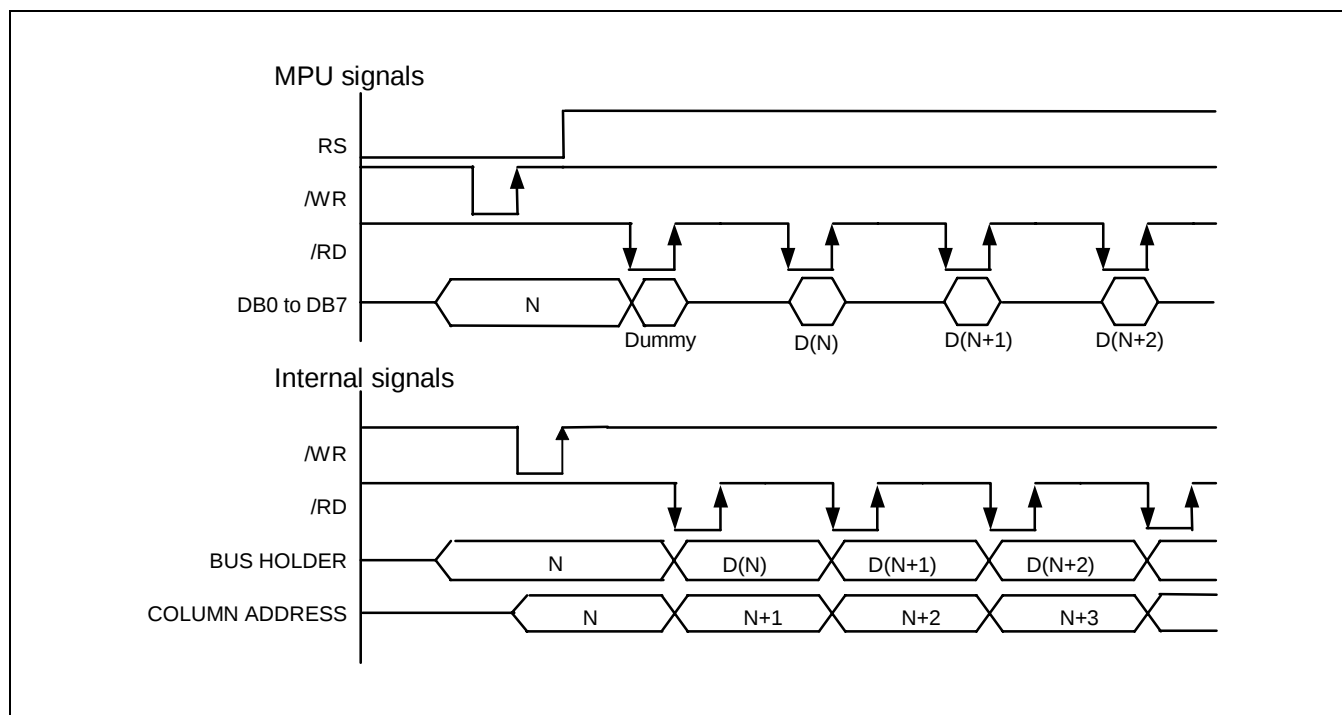
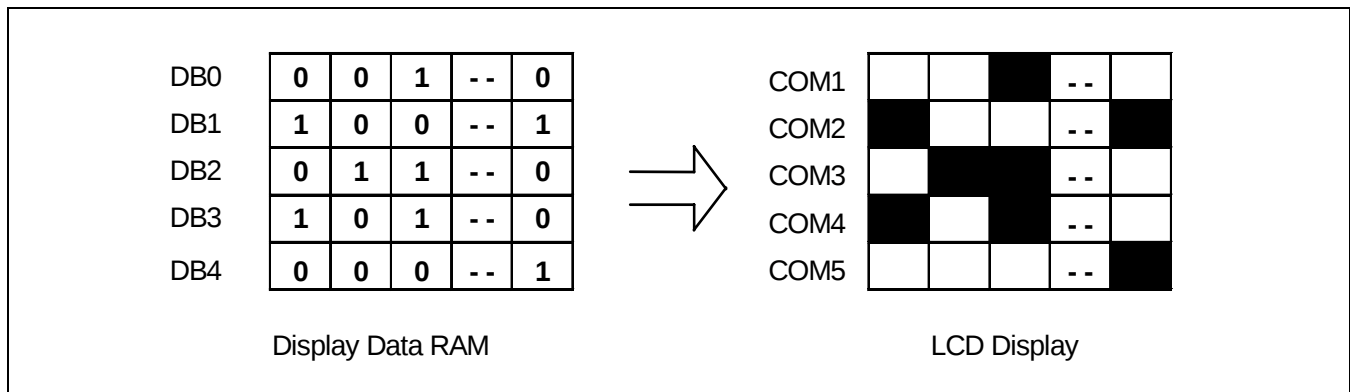


Figure 9. Read Timing

## DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 10. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.



**Figure 10. RAM-to-LCD Data Transfer**

### Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in Figure 12. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

### Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM1) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 12. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

### Column Address Circuit

Column address circuit has a 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 12. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a Read or Write Data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 11.

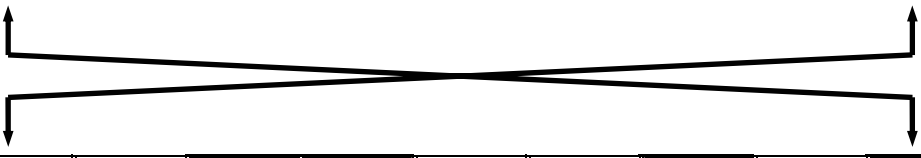
| SEG output                                                                          | SEG 1                                                                               | SEG 2                                                                               | SEG 3                                                                               | SEG 4                                                                               | ... .. | SEG 129                                                                               | SEG 130                                                                               | SEG 131                                                                               | SEG 132                                                                               |
|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Column address [Y7:Y0]                                                              | 00H                                                                                 | 01H                                                                                 | 02H                                                                                 | 03H                                                                                 | ... .. | 80H                                                                                   | 81H                                                                                   | 82H                                                                                   | 83H                                                                                   |
| Display data                                                                        | 1                                                                                   | 0                                                                                   | 1                                                                                   | 0                                                                                   |        | 1                                                                                     | 1                                                                                     | 0                                                                                     | 0                                                                                     |
| LCD panel display<br>( ADC = 0 )                                                    |    |    |    |    | ... .. |    |    |    |    |
|  |                                                                                     |                                                                                     |                                                                                     |                                                                                     |        |                                                                                       |                                                                                       |                                                                                       |                                                                                       |
| LCD panel display<br>( ADC = 1 )                                                    |  |  |  |  | ... .. |  |  |  |  |

Figure 11. The Relationship between the Column Address and the Segment Outputs

### Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, Reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

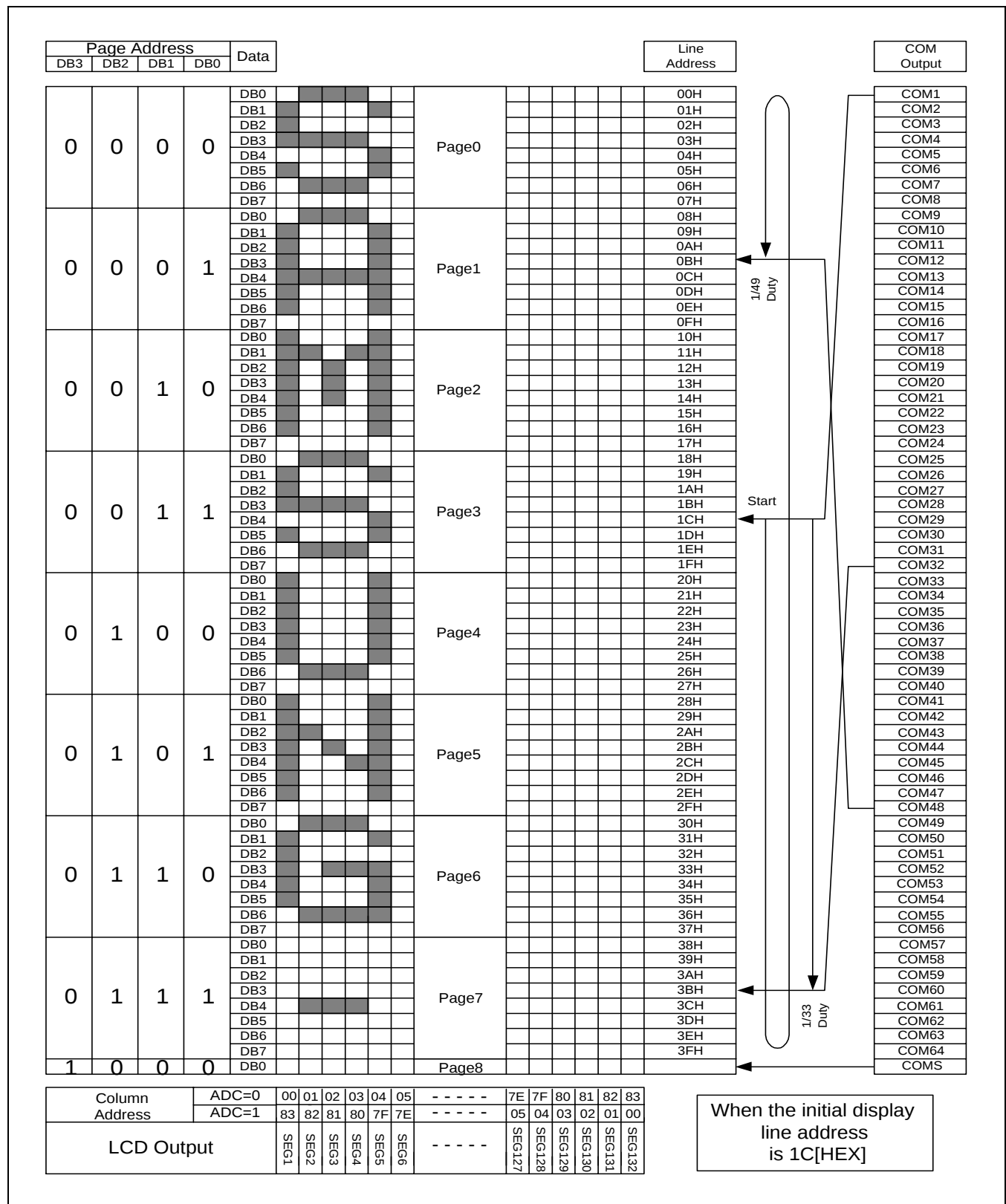


Figure 12. Display Data RAM Map

## LCD DISPLAY CIRCUITS

### Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of  $V_{DD}$ . This oscillator signal is used in the voltage converter and display timing generation circuit.

\* Test condition: Temperature: 25°C & 85°C, TEMPS="L", No load

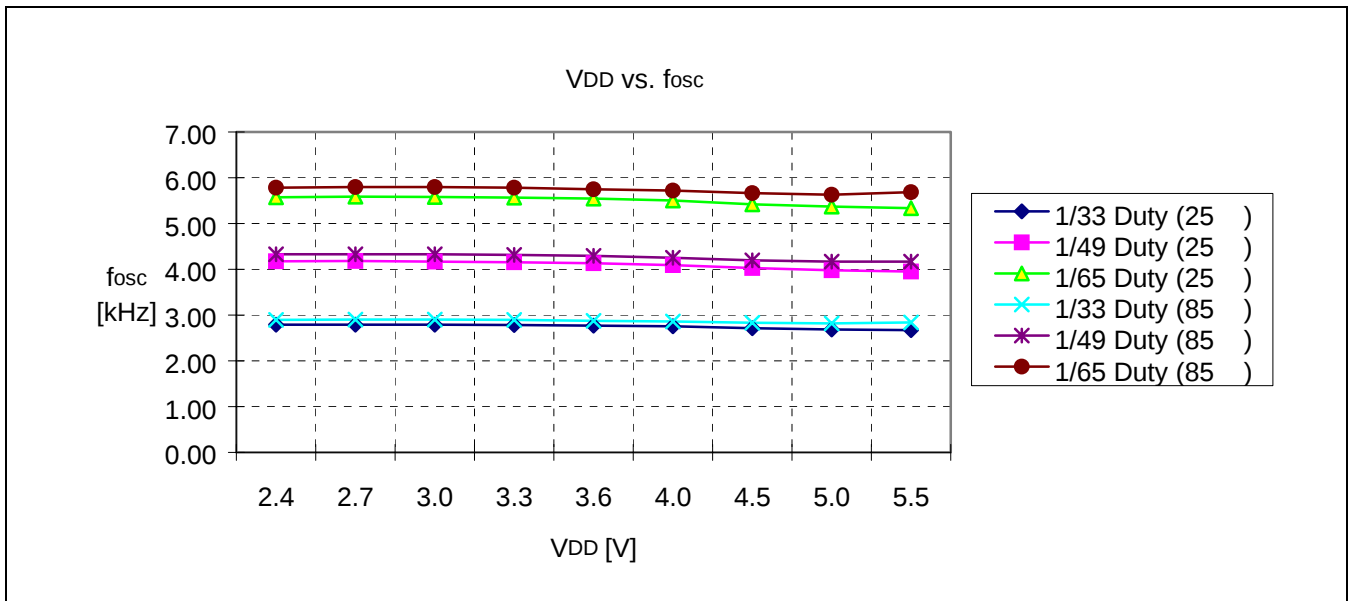


Figure 13.  $V_{DD}$  vs.  $f_{osc}$

### Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal(M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 14.

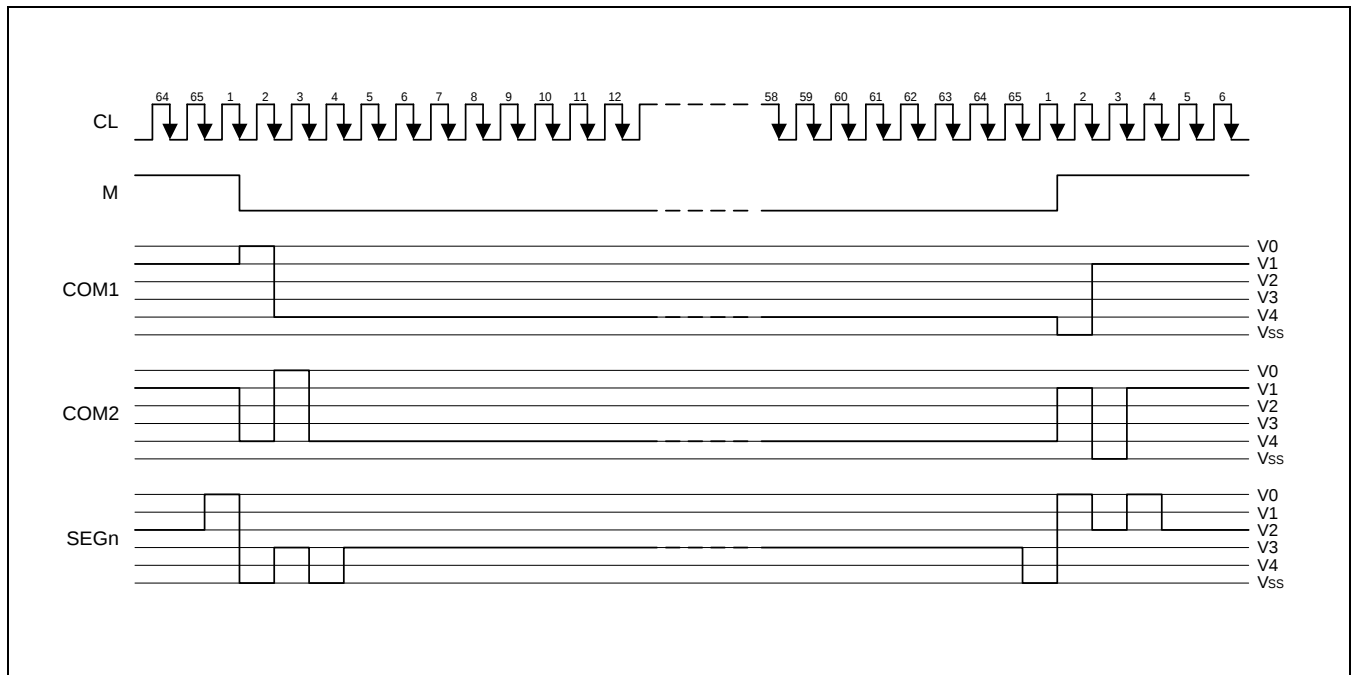


Figure 14. 2-frame AC Driving Waveform (Duty ratio = 1/65)

### Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 11. The Relationship between Duty Ratio and Common Output

| Duty | SHL | Common output pins |            |            |            |            |      |
|------|-----|--------------------|------------|------------|------------|------------|------|
|      |     | COM[1:16]          | COM[17:24] | COM[25:40] | COM[41:48] | COM[49:64] | COMS |
| 1/33 | 0   | COM[1:16]          | *NC        |            |            | COM[17:32] | COMS |
|      | 1   | COM[32:17]         | *NC        |            |            | COM[16:1]  |      |
| 1/49 | 0   | COM[1:24]          |            | *NC        | COM[25:48] |            | COMS |
|      | 1   | COM[48:25]         |            | *NC        | COM[24:1]  |            |      |
| 1/65 | 0   | COM[1:64]          |            |            |            |            | COMS |
|      | 1   | COM[64:1]          |            |            |            |            |      |

\*NC: No Connection

## LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel common drivers (including 2 COMS channels) and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

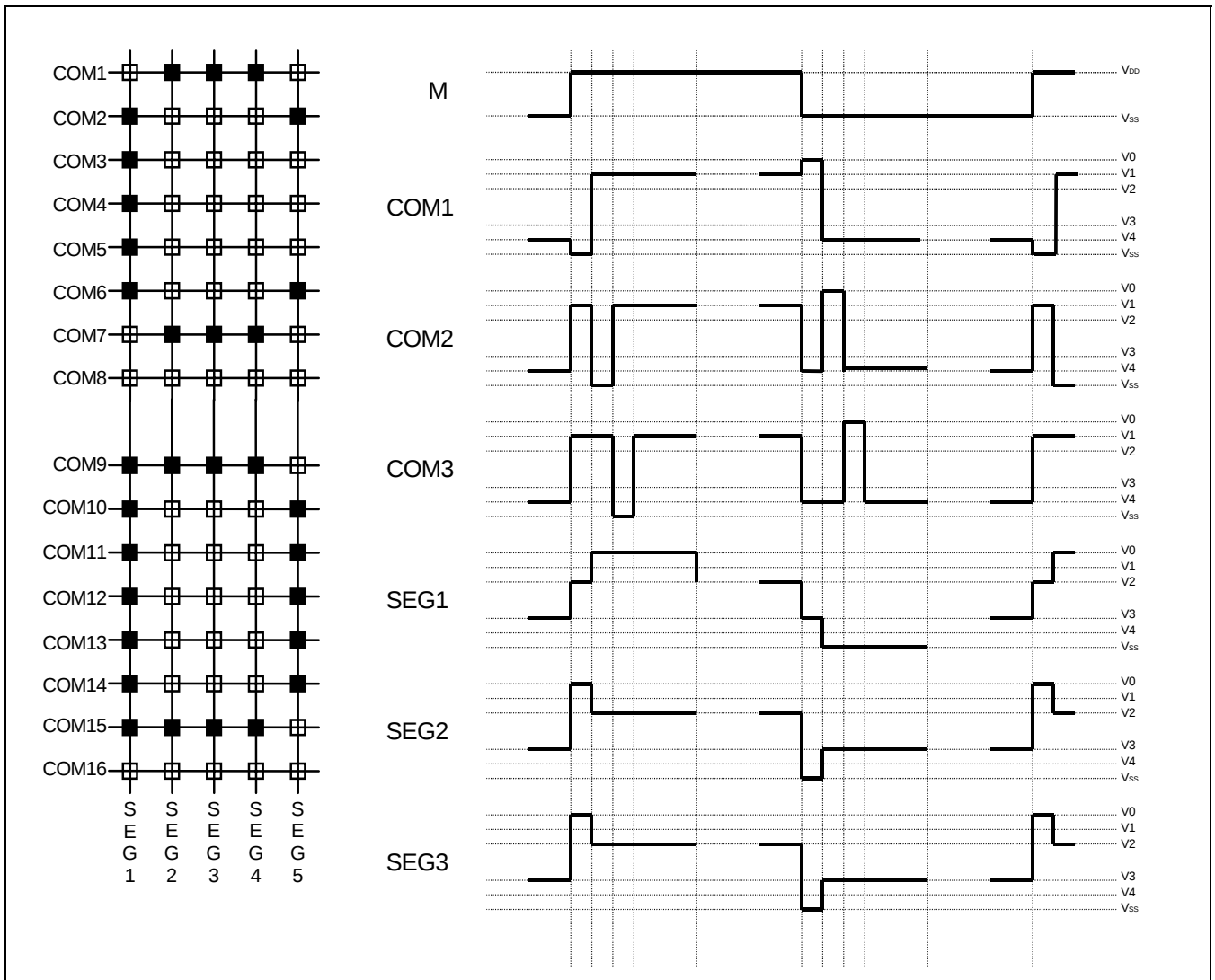


Figure 15. Segment and Common Timing

## POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using power supply circuits.

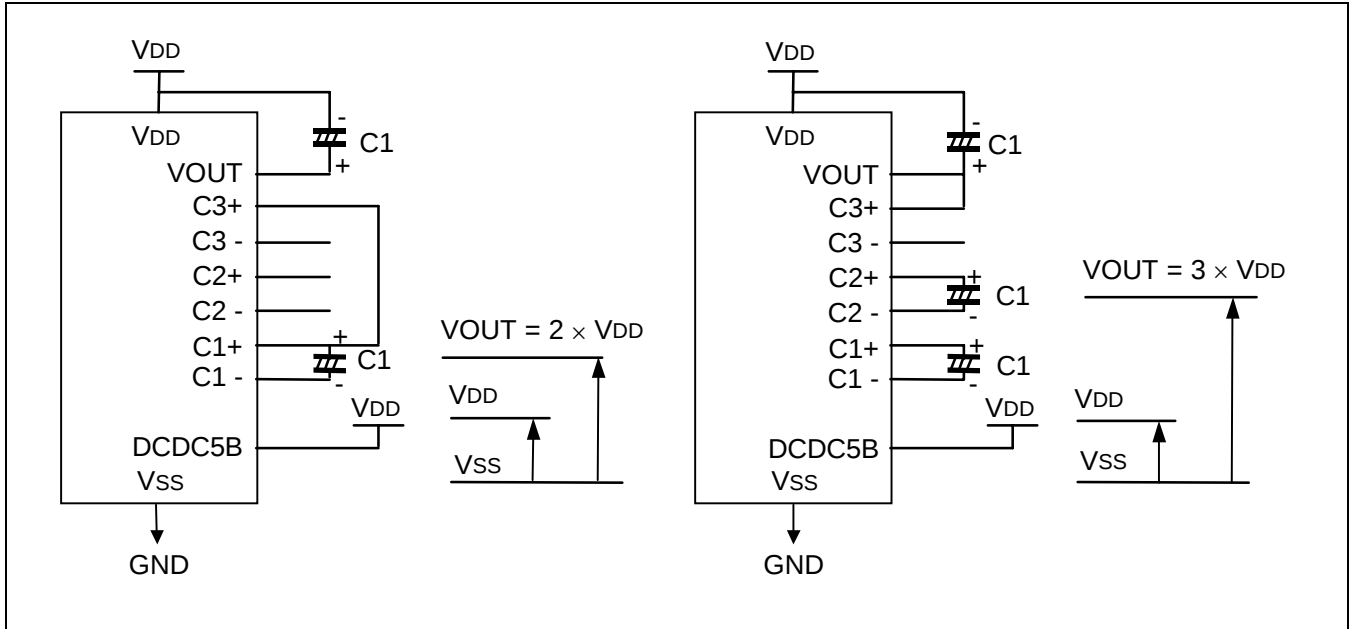
**Table 12. Recommended Power Supply Combinations**

| User setup                                                                 | Power control<br>(VC VR VF) | V/C<br>circuits | V/R<br>circuits | V/F<br>circuits | VOUT           | V0             | V1 to V4       |
|----------------------------------------------------------------------------|-----------------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|
| Only the internal power supply circuits are used                           | 1 1 1                       | ON              | ON              | ON              | Open           | Open           | Open           |
| Only the voltage regulator circuits and voltage follower circuits are used | 0 1 1                       | OFF             | ON              | ON              | External input | Open           | Open           |
| Only the voltage follower circuits are used                                | 0 0 1                       | OFF             | OFF             | ON              | Open           | External input | Open           |
| Only the external power supply circuits are used                           | 0 0 0                       | OFF             | OFF             | OFF             | Open           | External input | External input |

## Voltage Converter Circuits

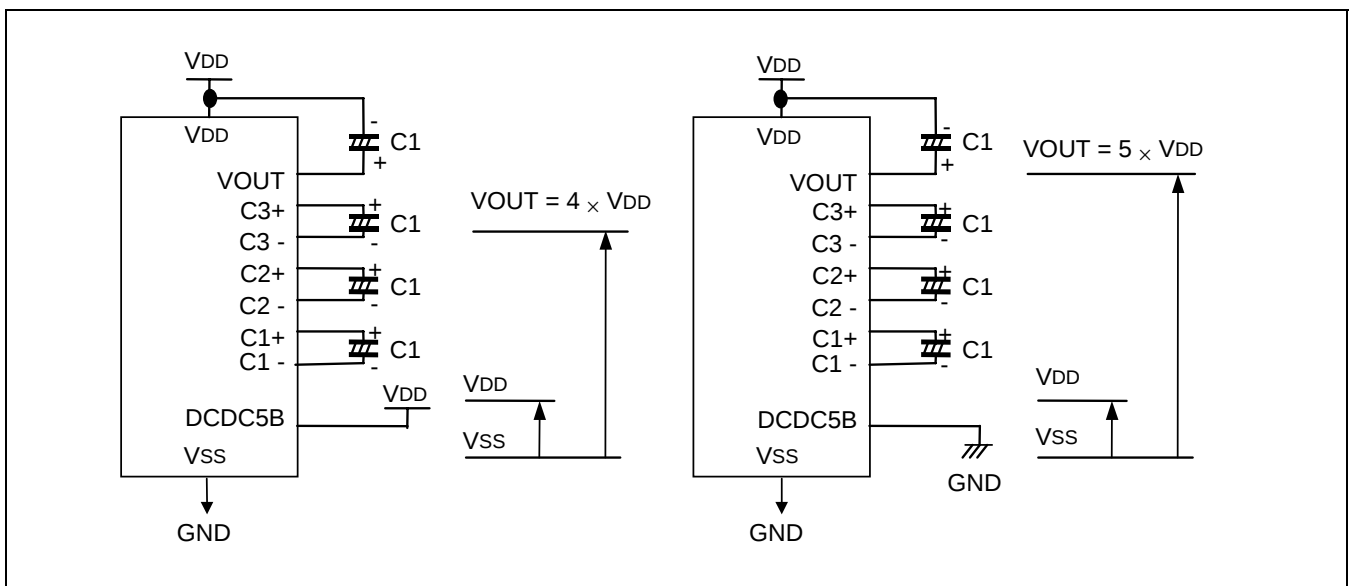
These circuits boost up the electric potential between VDD and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7  $\mu$ F]



### Figure 16. Two Times Boosting Circuit

### Figure 17. Three Times Boosting Circuit



**Figure 18. Four Times Boosting Circuit**

**Figure 19. Five Times Boosting Circuit**

### Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage,  $V_0$ , by adjusting resistors,  $R_a$  and  $R_b$ , within the range of  $|V_0| < |V_{OUT}|$ . Because  $V_{OUT}$  is the operating voltage of operational-amplifier circuits shown in figure 20, it is necessary to be applied internally or externally.

For the Eq. 1, we determine  $V_0$  by  $R_a$ ,  $R_b$  and  $V_{EV}$ . The  $R_a$  and  $R_b$  are connected internally or externally by INTR pin. And  $V_{EV}$  called the voltage of electronic volume is determined by Eq. 2, where the parameter  $\alpha$  is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63.  $V_{REF}$  voltage at  $T_a = 25^\circ\text{C}$  is shown in table 13.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad [\text{V}] \quad \text{----- (Eq. 1)}$$

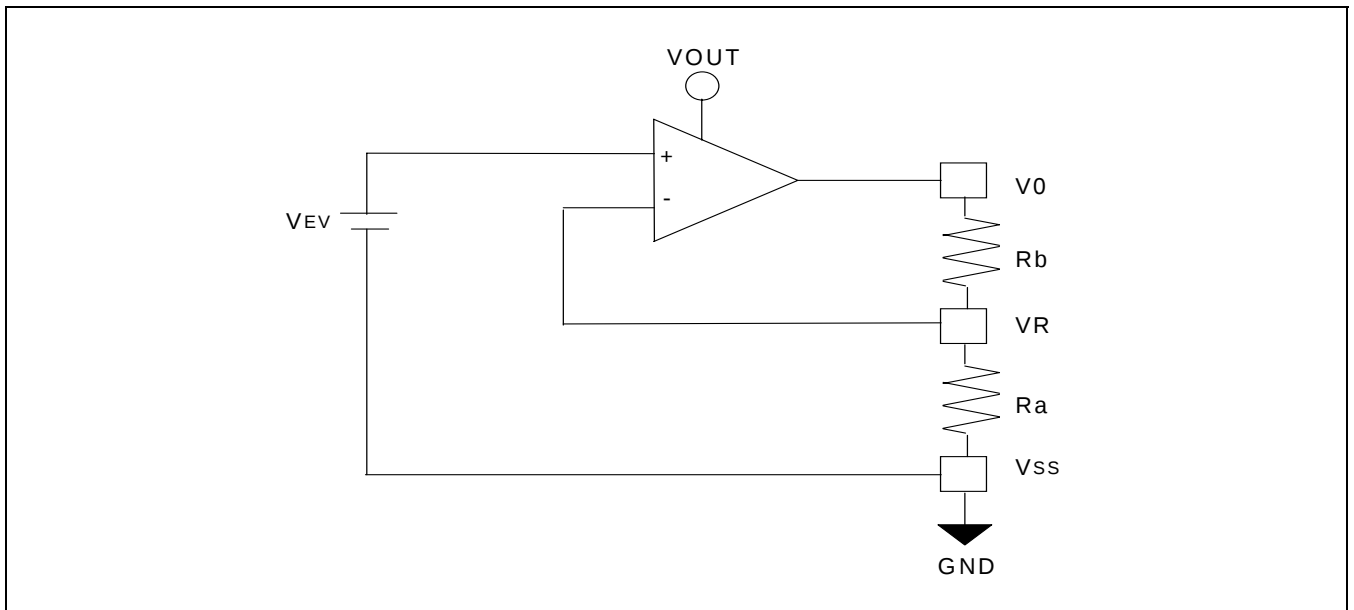
$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times V_{REF} \quad [\text{V}] \quad \text{----- (Eq. 2)}$$

**Table 13.  $V_{REF}$  Voltage at  $T_a = 25^\circ\text{C}$**

| TEMPS | Temp. coefficient         | $V_{REF}$ [V] |
|-------|---------------------------|---------------|
| L     | -0.05% / $^\circ\text{C}$ | 2.0           |
| H     | -0.2% / $^\circ\text{C}$  | 2.0           |

**Table 14. Reference Voltage Parameters ( $\alpha$ )**

| SV5 | SV4 | SV3 | SV2 | SV1 | SV0 | Reference voltage parameter ( $\alpha$ ) |
|-----|-----|-----|-----|-----|-----|------------------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0                                        |
| 0   | 0   | 0   | 0   | 0   | 1   | 1                                        |
| :   | :   | :   | :   | :   | :   | :                                        |
| :   | :   | :   | :   | :   | :   | :                                        |
| 1   | 1   | 1   | 1   | 1   | 0   | 62                                       |
| 1   | 1   | 1   | 1   | 1   | 1   | 63                                       |

**Figure 20. Internal Voltage Regulator Circuit**

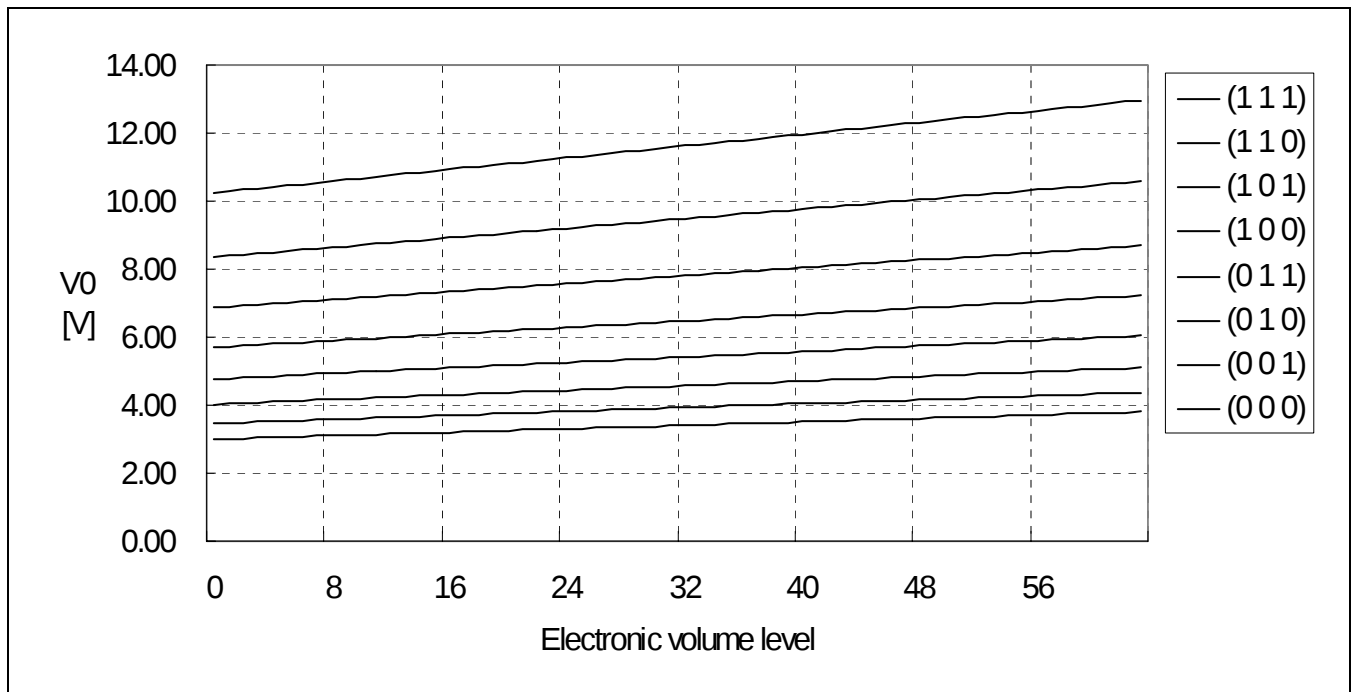
### In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

**Table 15. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)**

|               | 3-bit data settings (R2 R1 R0) |       |       |       |       |       |       |       |
|---------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|
|               | 0 0 0                          | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
| $1+(Rb / Ra)$ | 1.90                           | 2.19  | 2.55  | 3.02  | 3.61  | 4.35  | 5.29  | 6.48  |

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.



**Figure 21. Electronic Volume Level**

**In Case of Using External Resistors, Ra and Rb. (INTRS = "L")**

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and Vss, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA
4. Temperature coefficient = -0.05% / °C

From Eq. 1

$$10 = \left( 1 + \frac{R_b}{R_a} \right) \times V_{EV} \quad [V] \text{ ----- (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left( 1 - \frac{(63 - 32)}{300} \right) \times 2.0 = 1.79 \quad [V] \text{ ----- (Eq. 4)}$$

From requirement 3.

$$\frac{10}{R_a + R_b} = 1 \text{ [uA]} \text{ ----- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

$$R_a = 1.79 \text{ [M}\Omega\text{]}$$

$$R_b = 8.21 \text{ [M}\Omega\text{]}$$

The following table shows the range of V0 depending on the above requirements.

**Table 16. V0 Depending on Electronic Volume Level**

|    | Electronic volume level |       |       |       |       |
|----|-------------------------|-------|-------|-------|-------|
|    | 0                       | ..... | 32    | ..... | 63    |
| V0 | 8.83                    | ..... | 10.00 | ..... | 11.17 |

### Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

**Table 17. The Relationship between V1 to V4 level and Duty Ratio**

| Duty Ratio | DUTY1 | DUTY0 | LCD Bias | V1                | V2                | V3                | V4                |
|------------|-------|-------|----------|-------------------|-------------------|-------------------|-------------------|
| 1/33       | L     | L     | 1/5      | $(4/5) \times V0$ | $(3/5) \times V0$ | $(2/5) \times V0$ | $(1/5) \times V0$ |
|            |       |       | 1/6      | $(5/6) \times V0$ | $(4/6) \times V0$ | $(2/6) \times V0$ | $(1/6) \times V0$ |
| 1/49       | L     | H     | 1/6      | $(5/6) \times V0$ | $(4/6) \times V0$ | $(2/6) \times V0$ | $(1/6) \times V0$ |
|            |       |       | 1/8      | $(7/8) \times V0$ | $(6/8) \times V0$ | $(2/8) \times V0$ | $(1/8) \times V0$ |
| 1/65       | H     | L/H   | 1/7      | $(6/7) \times V0$ | $(5/7) \times V0$ | $(2/7) \times V0$ | $(1/7) \times V0$ |
|            |       |       | 1/9      | $(8/9) \times V0$ | $(7/9) \times V0$ | $(2/9) \times V0$ | $(1/9) \times V0$ |

## REFERECE CIRCUIT EXAMPLES

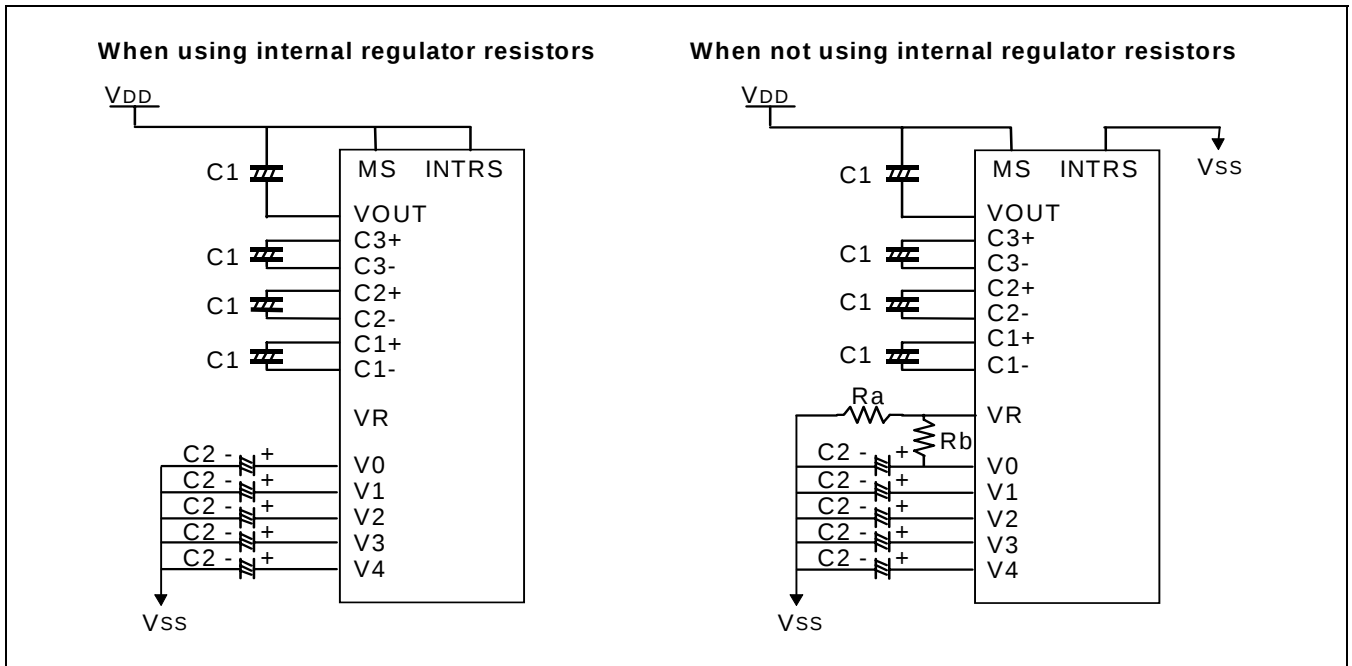


Figure 22. When Using all LCD Power Circuits (4-Time V/C: ON, V/R: ON, V/F: ON)

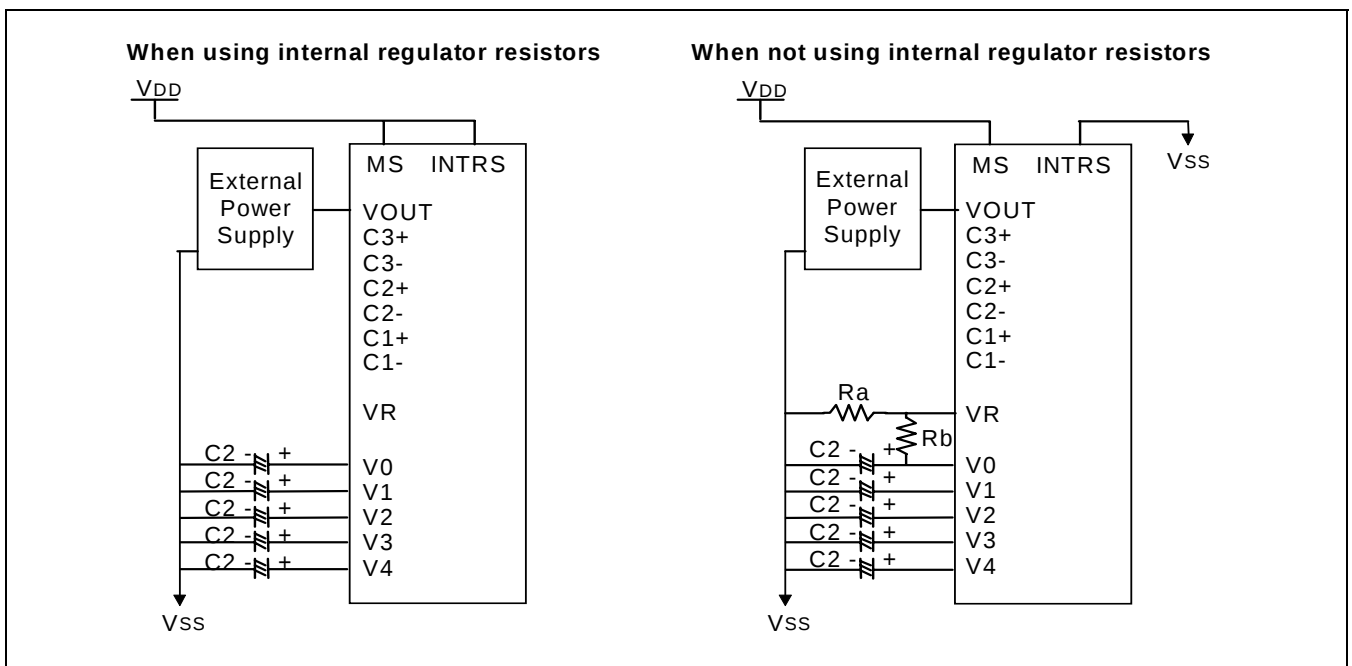


Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

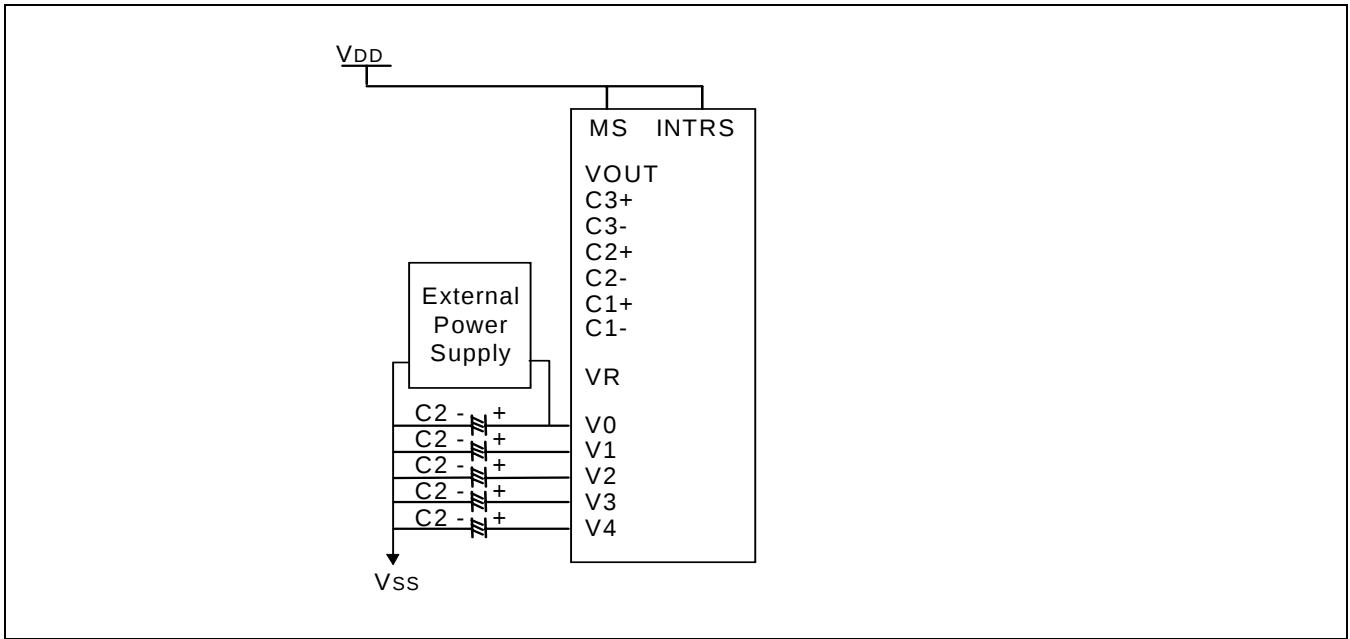


Figure 24. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

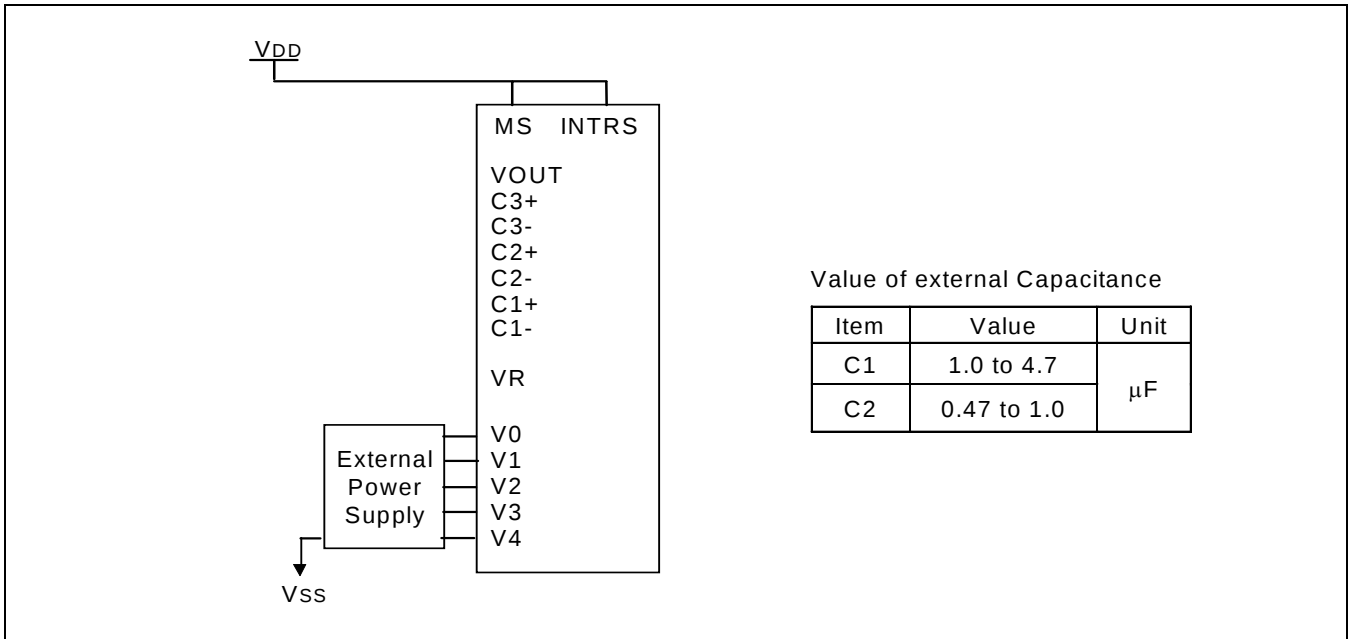


Figure 25. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

## RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.  
When RESETB becomes "L", following procedure is occurred.

Display ON / OFF: OFF  
Entire display ON / OFF: OFF (normal)  
ADC select: OFF (normal)  
Reverse display ON / OFF: OFF (normal)  
Power control register (VC, VR, VF) = (0, 0, 0)  
LCD bias ratio: 1/7 (1/65 duty), 1/6 (1/49 duty), 1/5 (1/33 duty)  
Read-modify-write: OFF  
SHL select: OFF (normal)  
Static indicator mode: OFF  
Static indicator register: (S1, S0) = (0, 0)  
Display start line: 0 (first)  
Column address: 0  
Page address: 0  
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)  
Reference voltage set: OFF  
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF  
Static indicator mode: OFF  
Static indicator register: (S1, S0) = (0, 0)  
SHL select: 0  
Display start line: 0 (first)  
Column address: 0  
Page address: 0  
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)  
Reference voltage set: OFF  
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is "L" or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

## INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don't care

| Instruction                    | RS | RW | DB7        | DB6 | DB5   | DB4    | DB3 | DB2 | DB1 | DB0  | Description                                                                                                                  |
|--------------------------------|----|----|------------|-----|-------|--------|-----|-----|-----|------|------------------------------------------------------------------------------------------------------------------------------|
| Read display data              | 1  | 1  | Read data  |     |       |        |     |     |     |      | Read data from DDRAM                                                                                                         |
| Write display data             | 1  | 0  | Write data |     |       |        |     |     |     |      | Write data into DDRAM                                                                                                        |
| Read status                    | 0  | 1  | BUSY       | ADC | ONOFF | RESETB | 0   | 0   | 0   | 0    | Read the internal status                                                                                                     |
| Display ON / OFF               | 0  | 0  | 1          | 0   | 1     | 0      | 1   | 1   | 1   | DON  | Turn on/off LCD panel<br>When DON = 0: display OFF<br>When DON = 1: display ON                                               |
| Initial display line           | 0  | 0  | 0          | 1   | ST5   | ST4    | ST3 | ST2 | ST1 | ST0  | Specify DDRAM line for COM1                                                                                                  |
| Set reference voltage mode     | 0  | 0  | 1          | 0   | 0     | 0      | 0   | 0   | 0   | 1    | Set reference voltage Mode                                                                                                   |
| Set reference voltage register | 0  | 0  | ×          | ×   | SV5   | SV4    | SV3 | SV2 | SV1 | SV0  | Set reference voltage register                                                                                               |
| Set page address               | 0  | 0  | 1          | 0   | 1     | 1      | P3  | P2  | P1  | P0   | Set page address                                                                                                             |
| Set column address MSB         | 0  | 0  | 0          | 0   | 0     | 1      | Y7  | Y6  | Y5  | Y4   | Set column address MSB                                                                                                       |
| Set column address LSB         | 0  | 0  | 0          | 0   | 0     | 0      | Y3  | Y2  | Y1  | Y0   | Set column address LSB                                                                                                       |
| ADC select                     | 0  | 0  | 1          | 0   | 1     | 0      | 0   | 0   | 0   | ADC  | Select SEG output direction<br>When ADC = 0: normal direction (SEG1→SEG132)<br>When ADC = 1: reverse direction (SEG132→SEG1) |
| Reverse display ON / OFF       | 0  | 0  | 1          | 0   | 1     | 0      | 0   | 1   | 1   | REV  | Select normal / reverse display<br>When REV = 0: normal display<br>When REV = 1: reverse display                             |
| Entire display ON / OFF        | 0  | 0  | 1          | 0   | 1     | 0      | 0   | 1   | 0   | EON  | Select normal / entire display ON<br>When EON = 0: normal display.<br>When EON = 1: entire display ON                        |
| LCD bias select                | 0  | 0  | 1          | 0   | 1     | 0      | 0   | 0   | 1   | BIAS | Select LCD bias                                                                                                              |
| Set modify-read                | 0  | 0  | 1          | 1   | 1     | 0      | 0   | 0   | 0   | 0    | Set modify-read mode                                                                                                         |
| Reset modify-read              | 0  | 0  | 1          | 1   | 1     | 0      | 1   | 1   | 1   | 0    | Release modify-read mode                                                                                                     |
| Reset                          | 0  | 0  | 1          | 1   | 1     | 0      | 0   | 0   | 1   | 0    | Initialize the internal functions                                                                                            |
| SHL select                     | 0  | 0  | 1          | 1   | 0     | 0      | SHL | ×   | ×   | ×    | Select COM output direction<br>When SHL = 0: normal direction (COM1→COM64)<br>When SHL = 1: reverse direction (COM64→COM1)   |
| Power control                  | 0  | 0  | 0          | 0   | 1     | 0      | 1   | VC  | VR  | VF   | Control power circuit operation                                                                                              |
| Regulator resistor select      | 0  | 0  | 0          | 0   | 1     | 0      | 0   | R2  | R1  | R0   | Select internal resistance ratio of the regulator resistor                                                                   |
| Set static indicator mode      | 0  | 0  | 1          | 0   | 1     | 0      | 1   | 1   | 0   | SM   | Set static indicator mode                                                                                                    |
| Set static indicator register  | 0  | 0  | ×          | ×   | ×     | ×      | ×   | ×   | S1  | S0   | Set static indicator register                                                                                                |
| Power save                     | -  | -  | -          | -   | -     | -      | -   | -   | -   | -    | Compound instruction of display OFF and entire display ON                                                                    |
| Test instruction               | 0  | 0  | 1          | 1   | 1     | 1      | ×   | ×   | ×   | ×    | <b><u>Don't use this instruction.</u></b>                                                                                    |

"x" : don't care

### Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

| RS | RW | DB7       | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----------|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1  | Read data |     |     |     |     |     |     |     |

### Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

| RS | RW | DB7        | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------------|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0  | Write data |     |     |     |     |     |     |     |

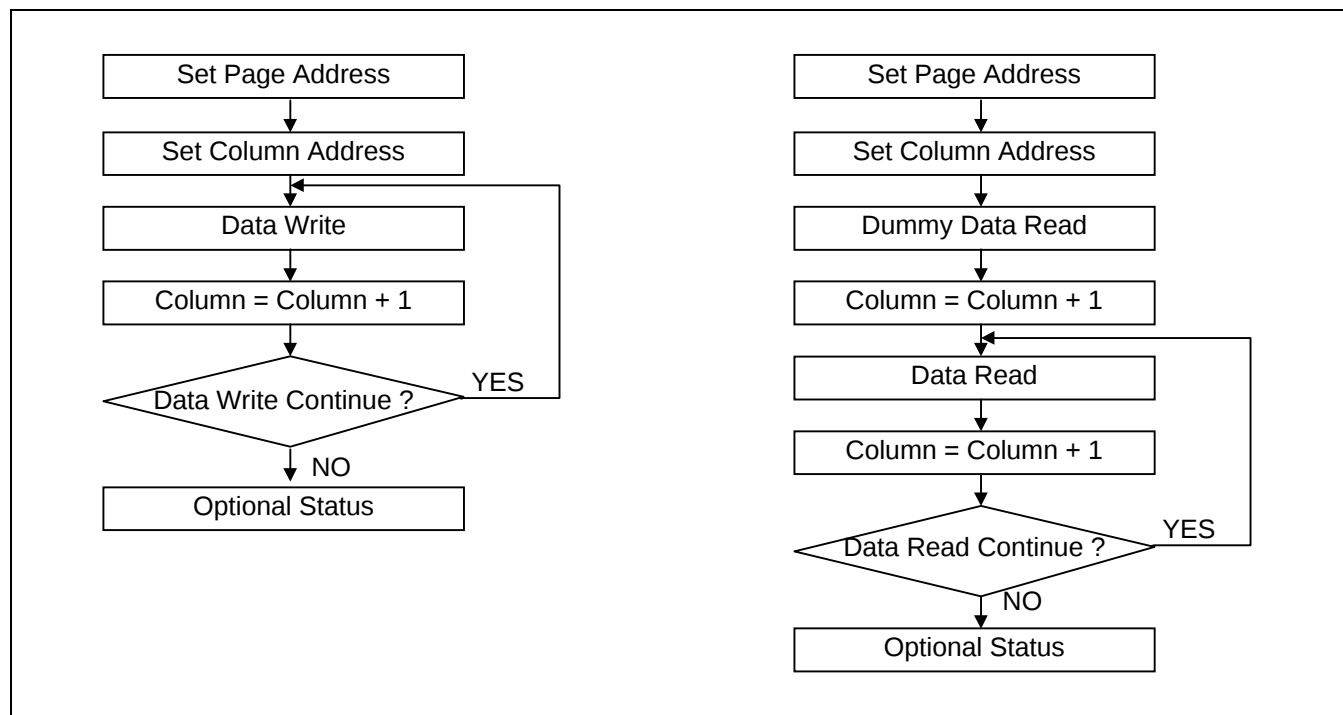


Figure 26. Sequence for Writing Display Data

Figure 27. Sequence for Reading Display Data

**Read Status**

Indicates the internal status of the S6B1713.

| RS | RW | DB7  | DB6 | DB5    | DB4    | DB3 | DB2 | DB1 | DB0 |
|----|----|------|-----|--------|--------|-----|-----|-----|-----|
| 0  | 1  | BUSY | ADC | ON/OFF | RESETB | 0   | 0   | 0   | 0   |

| Flag     | Description                                                                                                                                            |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| BUSY     | The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low.<br>0: chip is active, 1: chip is being busy.     |
| ADC      | Indicates the relationship between RAM column address and segment driver.<br>1: reverse direction (SEG132 → SEG1), 0: normal direction (SEG1 → SEG132) |
| ON / OFF | Indicates display ON / OFF status<br>0: display ON, 1: display OFF                                                                                     |
| RESETB   | Indicates the initialization is in progress by RESETB signal.<br>0: chip is active, 1: chip is being reset.                                            |

**Display ON / OFF**

Turns the display ON or OFF

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 1   | 1   | 1   | DON |

DON = 1: display ON

DON = 0: display OFF

**Initial Display Line**

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM1 when SHL = L, COM64 when SHL = H) of LCD panel.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 |

| ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | Line address |
|-----|-----|-----|-----|-----|-----|--------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0            |
| 0   | 0   | 0   | 0   | 0   | 1   | 1            |
| :   | :   | :   | :   | :   | :   | :            |
| 1   | 1   | 1   | 1   | 1   | 0   | 62           |
| 1   | 1   | 1   | 1   | 1   | 1   | 63           |

### Reference Voltage Select

Consists of 2-byte instruction

The 1<sup>st</sup> instruction sets reference voltage mode, the 2<sup>nd</sup> one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

#### The 1<sup>st</sup> Instruction: Set Reference Voltage Select Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

#### The 2<sup>nd</sup> Instruction: Set Reference Voltage Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | ×   | SV5 | SV4 | SV3 | SV2 | SV1 | SV0 |

| SV5 | SV4 | SV3 | SV2 | SV1 | SV0 | Reference voltage parameter ( $\alpha$ ) |
|-----|-----|-----|-----|-----|-----|------------------------------------------|
| 0   | 0   | 0   | 0   | 0   | 0   | 0                                        |
| 0   | 0   | 0   | 0   | 0   | 1   | 1                                        |
| :   | :   | :   | :   | :   | :   | :                                        |
| :   | :   | :   | :   | :   | :   | :                                        |
| 1   | 1   | 1   | 1   | 1   | 0   | 62                                       |
| 1   | 1   | 1   | 1   | 1   | 1   | 63                                       |

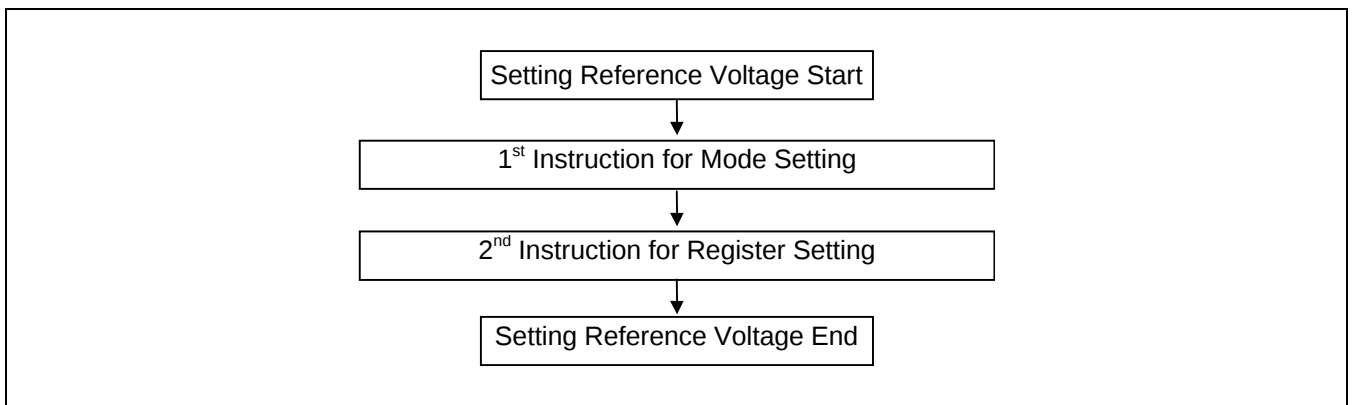


Figure 28. Sequence for Setting the Reference Voltage

**Set Page Address**

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 1   | P3  | P2  | P1  | P0  |

| P3 | P2 | P1 | P0 | Page |
|----|----|----|----|------|
| 0  | 0  | 0  | 0  | 0    |
| 0  | 0  | 0  | 1  | 1    |
| :  | :  | :  | :  | :    |
| 0  | 1  | 1  | 1  | 7    |
| 1  | 0  | 0  | 0  | 8    |

**Set Column Address**

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

**Set Column Address MSB**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 0   | 1   | Y7  | Y6  | Y5  | Y4  |

**Set Column Address LSB**

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 0   | 0   | Y3  | Y2  | Y1  | Y0  |

| Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Column address |
|----|----|----|----|----|----|----|----|----------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1              |
| :  | :  | :  | :  | :  | :  | :  | :  | :              |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 130            |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 131            |

**ADC Select**

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 0   | ADC |

ADC = 0: normal direction (SEG1 → SEG132)

ADC = 1: reverse direction (SEG132 → SEG1)

**Reverse Display ON / OFF**

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 1   | 1   | REV |

| REV         | RAM bit data = "1"           | RAM bit data = "0"           |
|-------------|------------------------------|------------------------------|
| 0 (normal)  | LCD pixel is illuminated     | LCD pixel is not illuminated |
| 1 (reverse) | LCD pixel is not illuminated | LCD pixel is illuminated     |

**Entire Display ON / OFF**

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 1   | 0   | EON |

EON = 0: normal display

EON = 1: entire display ON

**Select LCD Bias**

Selects LCD bias ratio of the voltage required for driving the LCD.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0  |
|----|----|-----|-----|-----|-----|-----|-----|-----|------|
| 0  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 1   | Bias |

| Duty ratio | DUTY1 | DUTY0 | LCD bias |          |
|------------|-------|-------|----------|----------|
|            |       |       | Bias = 0 | Bias = 1 |
| 1/33       | 0     | 0     | 1/5      | 1/6      |
| 1/49       | 0     | 1     | 1/6      | 1/8      |
| 1/65       | 1     | 0/1   | 1/7      | 1/9      |

### Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 0   |

### Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 1   | 1   | 1   | 0   |

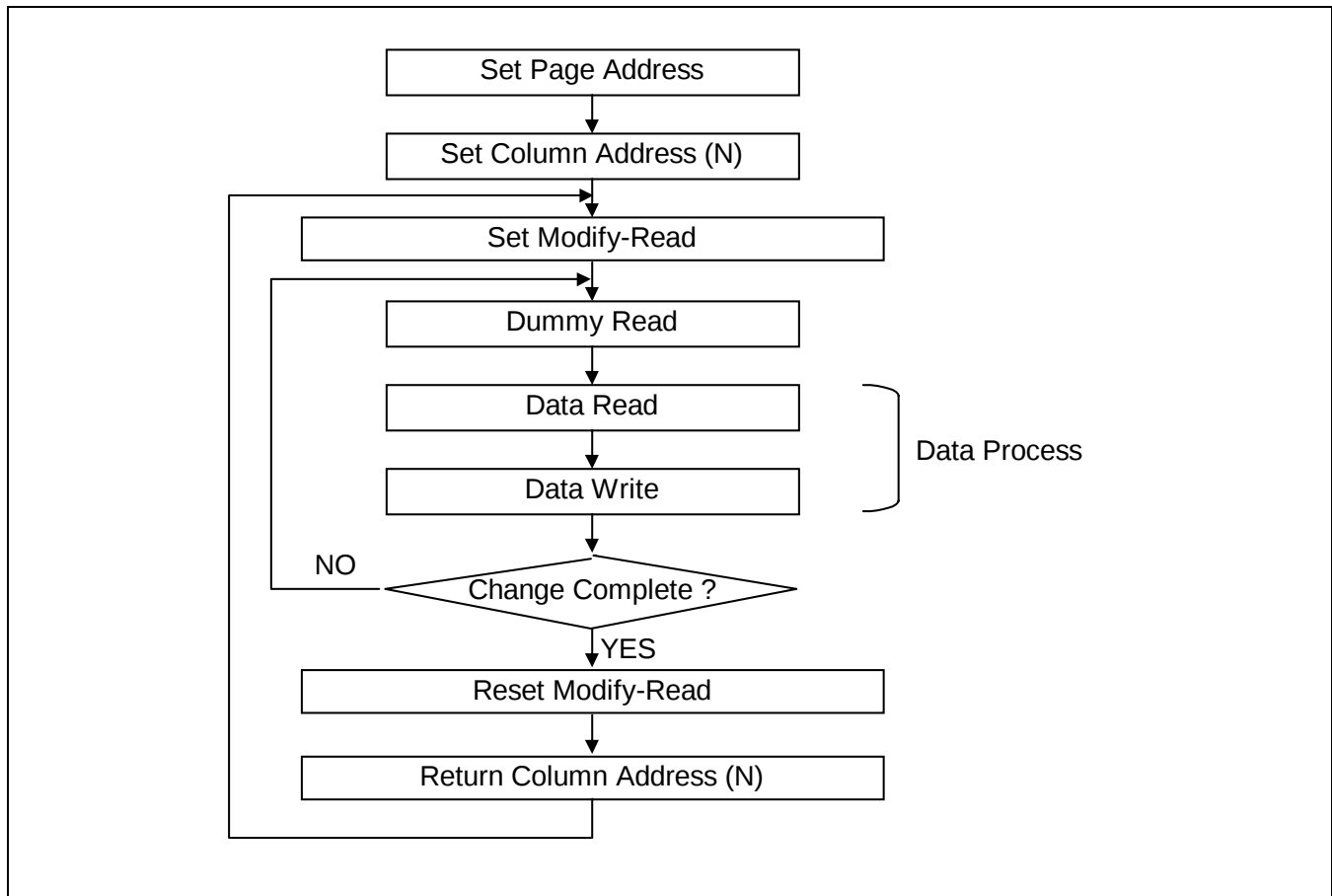


Figure 29. Sequence for Cursor Display

**Reset**

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 1   | 0   | 0   | 0   | 1   | 0   |

**SHL Select**

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 1   | 0   | 0   | SHL | ×   | ×   | ×   |

× : Don't care

SHL = 0: normal direction (COM1 → COM64)

SHL = 1: reverse direction (COM64 → COM1)

**Power control**

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 1   | 0   | 1   | VC  | VR  | VF  |

| VC | VR | VF | Status of internal power supply circuits  |
|----|----|----|-------------------------------------------|
| 0  |    |    | Internal voltage converter circuit is OFF |
| 1  |    |    | Internal voltage converter circuit is ON  |
|    | 0  |    | Internal voltage regulator circuit is OFF |
|    | 1  |    | Internal voltage regulator circuit is ON  |
|    |    | 0  | Internal voltage follower circuit is OFF  |
|    |    | 1  | Internal voltage follower circuit is ON   |

### Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 0   | 1   | 0   | 0   | R2  | R1  | R0  |

| R2 | R1 | R0 | 1 + (Rb / Ra) |
|----|----|----|---------------|
| 0  | 0  | 0  | 1.90          |
| 0  | 0  | 1  | 2.19          |
| 0  | 1  | 0  | 2.55          |
| 0  | 1  | 1  | 3.02          |
| 1  | 0  | 0  | 3.61          |
| 1  | 0  | 1  | 4.35          |
| 1  | 1  | 0  | 5.29          |
| 1  | 1  | 1  | 6.48          |

### Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the static indicator ON / OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

#### The 1<sup>st</sup> Instruction: Set Static Indicator Mode (ON / OFF)

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | 0   | 1   | 0   | 1   | 1   | 0   | SM  |

SM = 0: static indicator OFF

SM = 1: static indicator ON

#### The 2<sup>nd</sup> Instruction: Set Static Indicator Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | ×   | ×   | ×   | ×   | ×   | ×   | S1  | S0  |

| S1 | S0 | Status of static indicator output |
|----|----|-----------------------------------|
| 0  | 0  | OFF                               |
| 0  | 1  | ON (about 1 second blinking)      |
| 1  | 0  | ON (about 0.5 second blinking )   |
| 1  | 1  | ON (always ON)                    |

### Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B1713 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON and entire display OFF instruction.

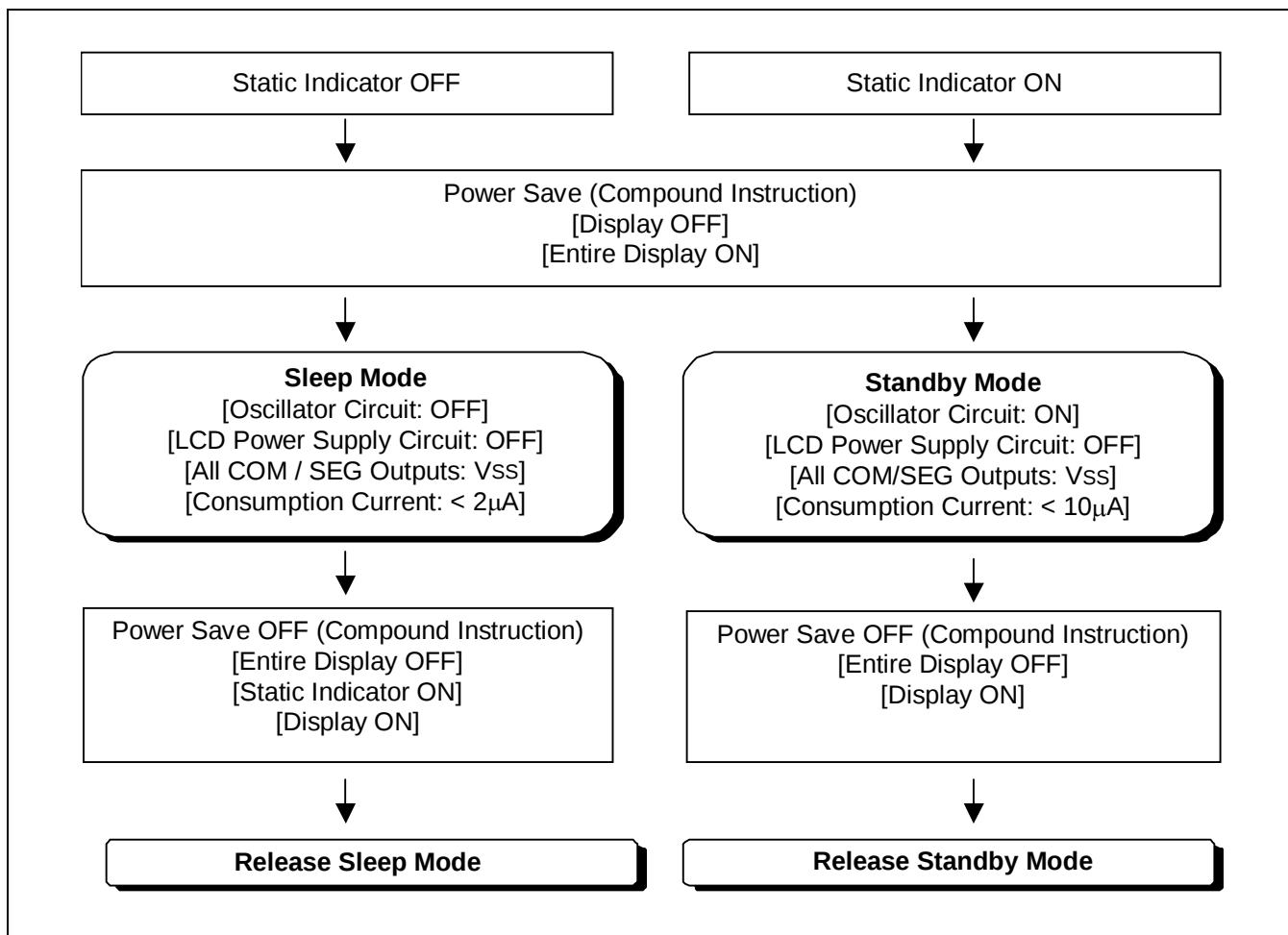


Figure 30. Power Save Routine

## Referential Instruction Setup Flow (1)

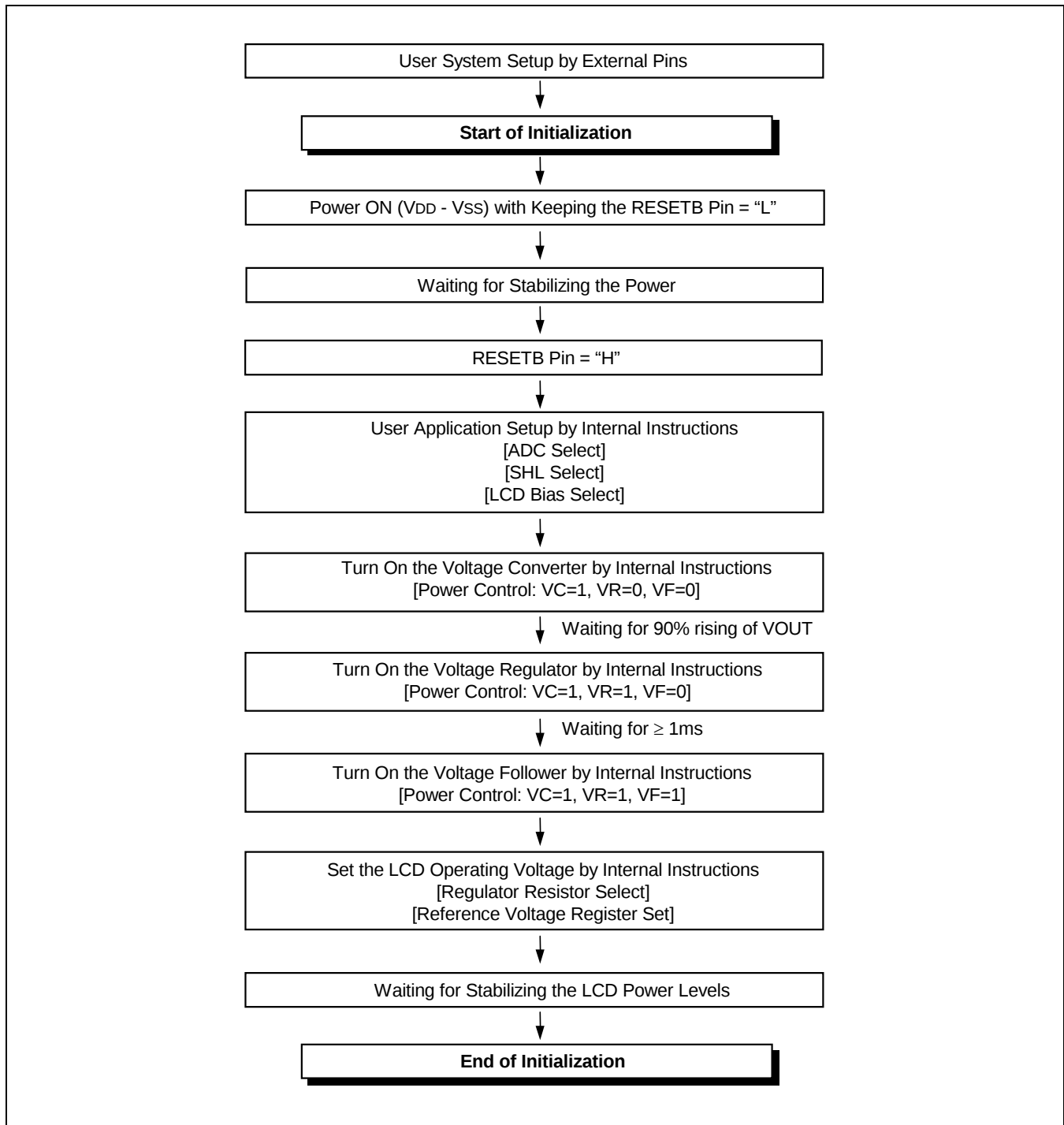


Figure 31. Initializing with the Built-in Power Supply Circuits

## Referential Instruction Setup Flow (2)

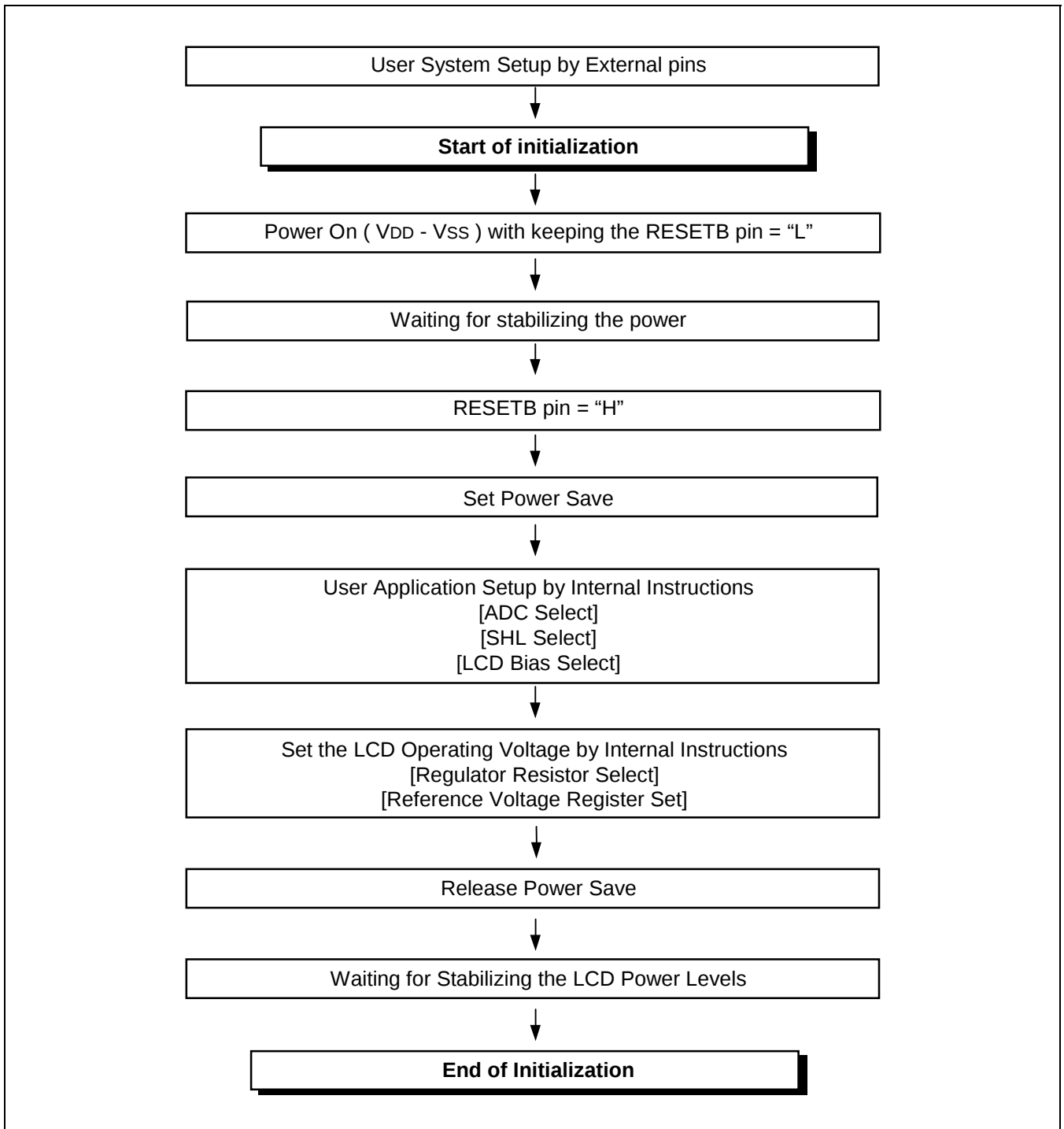


Figure 32. Initializing without the Built-in Power Supply Circuits

## Referential Instruction Setup Flow (3)

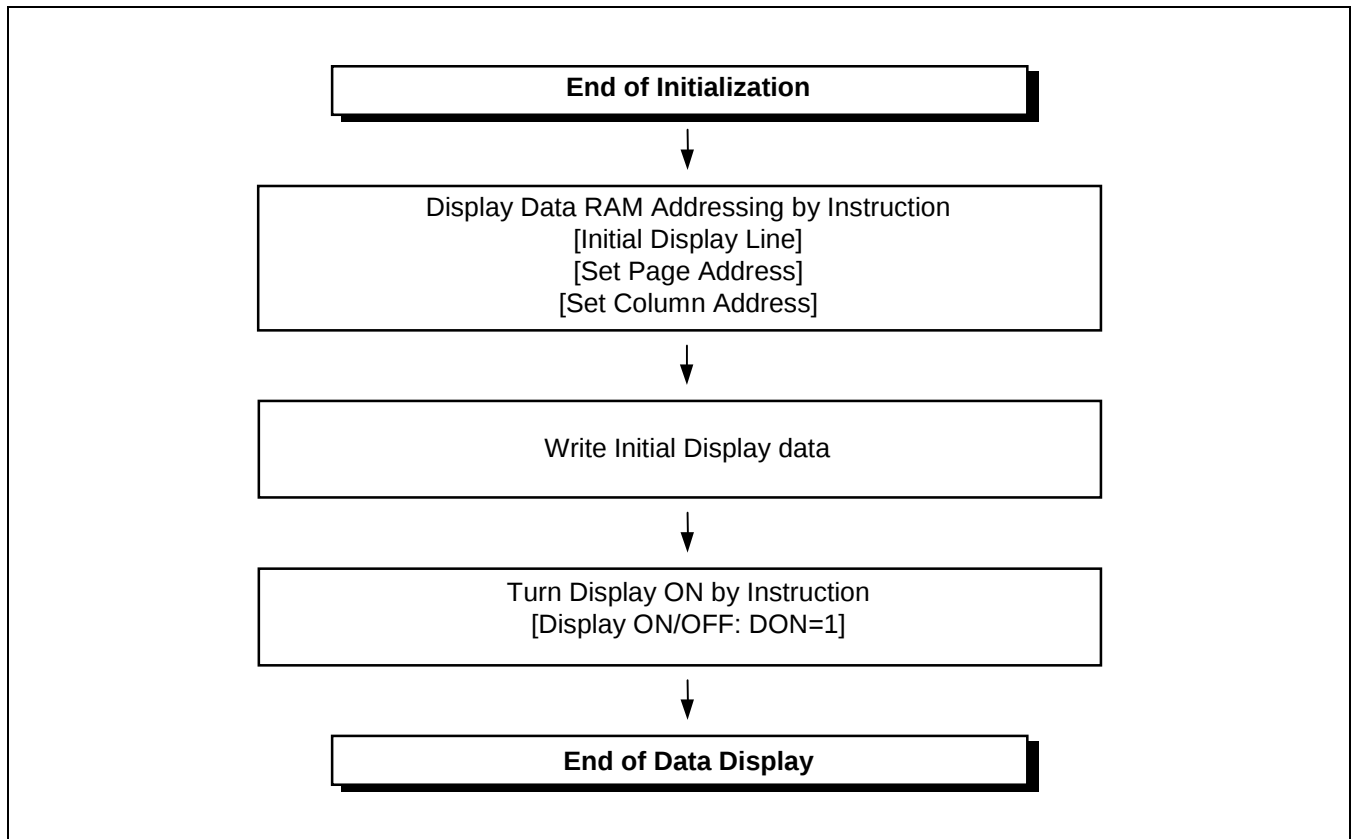


Figure 33. Data Displaying

## Referential Instruction Setup Flow (4)

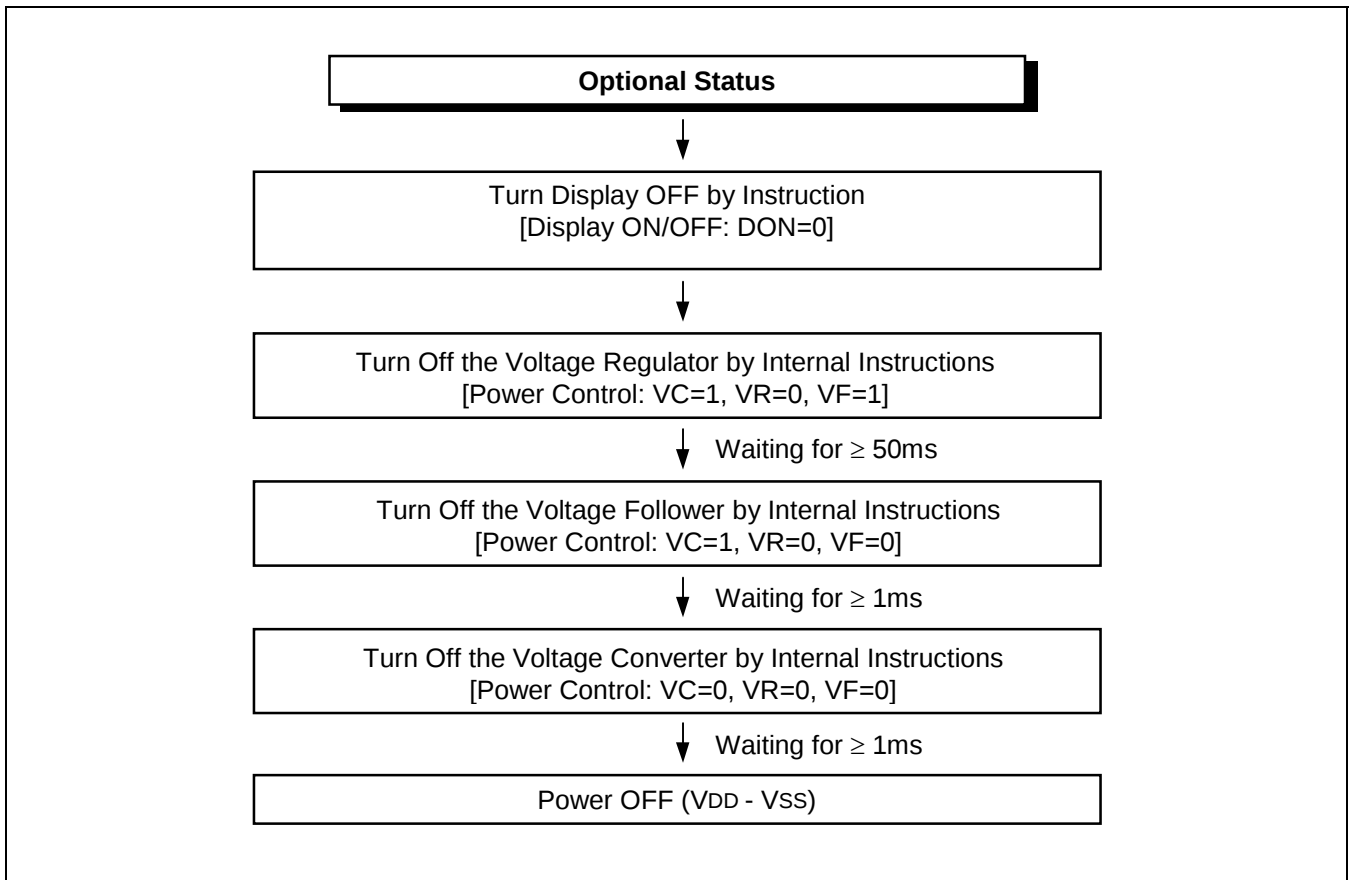


Figure 34. Power OFF

## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

| Parameter                   | Symbol           | Rating                       | Unit |
|-----------------------------|------------------|------------------------------|------|
| Supply voltage range        | V <sub>DD</sub>  | -0.3 to +7.0                 | V    |
|                             | V <sub>LCD</sub> | -0.3 to +17.0                | V    |
| Input voltage range         | V <sub>IN</sub>  | -0.3 to V <sub>DD</sub> +0.3 | V    |
| Operating temperature range | T <sub>OPR</sub> | -40 to +85                   | °C   |
| Storage temperature range   | T <sub>STR</sub> | -55 to +125                  | °C   |

NOTES:

1. V<sub>DD</sub> and V<sub>LCD</sub> are based on V<sub>SS</sub> = 0V.
2. Voltages V<sub>0</sub> ≥ V<sub>1</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>4</sub> ≥ V<sub>SS</sub> must always be satisfied. (V<sub>LCD</sub> = V<sub>0</sub> – V<sub>SS</sub>)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

## DC CHARACTERISTICS

Table 20. DC Characteristics

(VSS = 0V, VDD = 2.4 to 5.5V, Ta = -40 to 85°C)

| Item                                |          | Symbol     | Condition                                             | Min.   | Typ. | Max    | Unit | Pin used        |
|-------------------------------------|----------|------------|-------------------------------------------------------|--------|------|--------|------|-----------------|
| Operating voltage (1)               |          | VDD        | Select by product code                                | 2.4    | -    | 3.6    | V    | VDD *1          |
|                                     |          |            |                                                       | 2.4    | -    | 5.5    | V    |                 |
| Operating voltage (2)               |          | V0         |                                                       | 4.0    | -    | 15.0   | V    | V0 *2           |
| Input voltage                       | High     | VIH        |                                                       | 0.8VDD | -    | VDD    | V    | *3              |
|                                     | Low      | VIL        |                                                       | VSS    | -    | 0.2VDD |      |                 |
| Output voltage                      | High     | VOH        | IOH = -0.5mA                                          | 0.8VDD | -    | VDD    | V    | *4              |
|                                     | Low      | VOL        | IOL = 0.5mA                                           | VSS    | -    | 0.2VDD |      |                 |
| Input leakage current               |          | IIL        | VDD = 3.0V<br>VIN = VDD or VSS                        | - 1.0  | -    | + 1.0  | μA   | *5              |
| Output leakage current              |          | IOZ        | VIN = VDD or VSS                                      | - 3.0  | -    | + 3.0  | μA   | *6              |
| LCD driver ON resistance            |          | RON        | Ta = 25°C, V0 = 8V                                    | -      | 2.0  | 3.0    | KΩ   | SEgN<br>COMn *7 |
| Oscillator frequency (1)            | Internal | fOSC       | VDD = 3.0V<br>Ta = 25°C                               | 17     | 22   | 27     | kHz  | CL *8           |
|                                     | External | fCL        | Duty ratio = 1/65, 1/33                               | 4.25   | 5.50 | 6.75   |      |                 |
| Oscillator frequency (2)            | Internal | fOSC       | VDD = 3.0V<br>Ta = 25°C                               | 20     | 25   | 30     | kHz  | CL *8           |
|                                     | External | fCL        | Duty ratio = 1/49                                     | 3.33   | 4.17 | 5.00   |      |                 |
| Voltage converter input voltage     |          | VDD        | × 2                                                   | 2.4    | -    | 5.5    | V    | VDD             |
|                                     |          |            | × 3                                                   | 2.4    | -    | 5.0    |      |                 |
|                                     |          |            | × 4                                                   | 2.4    | -    | 3.75   |      |                 |
|                                     |          |            | × 5                                                   | 2.4    | -    | 3.0    |      |                 |
| Voltage converter output voltage    |          | VOUT       | ×2 / ×3 / ×4 / ×5<br>voltage conversion<br>(no-load ) | 95     | 99   | -      | %    | VOUT            |
| Voltage regulator operating voltage |          | VOUT       |                                                       | 4.0    | -    | 15.0   | V    | VOUT            |
| Voltage follower operating voltage  |          | V0         |                                                       | 4.0    | -    | 15.0   | V    | V0 *9           |
| Reference voltage                   | VREF0    | VDD = 3.0V | -0.05%/°C                                             | 1.94   | 2.00 | 2.06   | V    | *10             |
|                                     | VREF1    | Ta = 25°C  | -0.2%/°C                                              | 1.94   | 2.00 | 2.06   | V    | *10             |

**Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)**

(Ta = 25 °C)

| Item                            | Symbol           | Condition                                                                                                    | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|------------------|--------------------------------------------------------------------------------------------------------------|------|------|------|------|----------|
| Dynamic current consumption (1) | I <sub>DD1</sub> | V <sub>DD</sub> = 3.0V<br>V <sub>O</sub> – V <sub>SS</sub> = 11.0V<br>1/65 duty ratio<br>Display pattern OFF | -    | -    | 20   | μA   | *11      |

**Dynamic Current Consumption (2) when the built-in power circuit is ON (At operate mode)**

(Ta = 25 °C)

| Item                            | Symbol           | Condition                                                                                                                                                   | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|----------|
| Dynamic current consumption (2) | I <sub>DD2</sub> | V <sub>DD</sub> = 3.0V,<br>quad boosting,<br>V <sub>O</sub> – V <sub>SS</sub> = 11.0V,<br>1/65 duty ratio,<br>Display pattern OFF,<br>Normal power mode     | -    | 70   | 100  | μA   | *12      |
|                                 |                  | V <sub>DD</sub> = 3.0V,<br>quad boosting,<br>V <sub>O</sub> – V <sub>SS</sub> = 11.0V,<br>1/65 duty ratio,<br>Display pattern checker,<br>Normal power mode | -    | 95   | 160  | μA   | *12      |

**Current Consumption During Power Save Mode**

(Ta = 25 °C)

| Item                 | Symbol            | Condition                                | Min. | Typ. | Max. | Unit | Pin used |
|----------------------|-------------------|------------------------------------------|------|------|------|------|----------|
| Sleep mode current   | I <sub>DDS1</sub> | V <sub>DD</sub> = 3.0V<br>During sleep   | -    | -    | 2.0  | μA   |          |
| Standby mode current | I <sub>DDS2</sub> | V <sub>DD</sub> = 3.0V<br>During standby | -    | -    | 10.0 | μA   |          |

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

| Duty Ratio | Item                                   | f <sub>CL</sub>                   | f <sub>M</sub>                 |
|------------|----------------------------------------|-----------------------------------|--------------------------------|
| 1/65       | On-chip oscillator circuit is used     | $\frac{f_{osc}}{4}$               | $\frac{f_{osc}}{8 \times 65}$  |
|            | On-chip oscillator circuit is not used | External input (f <sub>CL</sub> ) | $\frac{f_{CL}}{2 \times 65}$   |
| 1/49       | On-chip oscillator circuit is used     | $\frac{f_{osc}}{6}$               | $\frac{f_{osc}}{12 \times 49}$ |
|            | On-chip oscillator circuit is not used | External input (f <sub>CL</sub> ) | $\frac{f_{CL}}{2 \times 49}$   |
| 1/33       | On-chip oscillator circuit is used     | $\frac{f_{osc}}{8}$               | $\frac{f_{osc}}{16 \times 33}$ |
|            | On-chip oscillator circuit is not used | External input (f <sub>CL</sub> ) | $\frac{f_{CL}}{2 \times 33}$   |

(f<sub>osc</sub>: oscillation frequency, f<sub>CL</sub>: display clock frequency, f<sub>M</sub>: LCD AC signal frequency)

[\* Remark Solves]

- \*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- \*2. In case of external power supply is applied.
- \*3. CS1B, CS2, RS, DB0 to DB7, E\_RD, RW\_WR, RESETB, MS, MI, PS, INTR, HPM, TEMPS, BSTS, DCDC5B, CLS pins.
- \*4. DB0 to DB7, M, FRS pins.
- \*5. CS1B, CS2, RS, DB [7:0], E\_RD, RW\_WR, RESETB, MS, MI, PS, INTR, HPM, TEMPS, BSTS, DCDC5B, CLS pins.
- \*6. Applies when the DB [7:0], M, DISP, and CL pins are in high impedance.
- \*7. Resistance value when  $\pm 0.1$ [mA] is applied during the ON status of the output pin SEG<sub>n</sub> or COM<sub>n</sub>.  
RON =  $\Delta V / 0.1$  [k $\Omega$ ] ( $\Delta V$ : voltage change when  $\pm 0.1$ [mA] is applied in the ON status.)
- \*8. See table 21 for the relationship between oscillation frequency and frame frequency.
- \*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
- \*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- \*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.  
The current consumption, when the built-in power supply circuit is ON or OFF.  
The current flowing through voltage regulation resistors (Ra and Rb) is not included.  
It does not include the current of the LCD panel capacity, wiring capacity, etc.

REFERENCE DATA

IDD1 vs. VDD

\* Test Condition: Temperature: 25°C & 85°C, V0 = 11V (External), TEMPS = 'L', 1/65 duty, Normal Power Mode

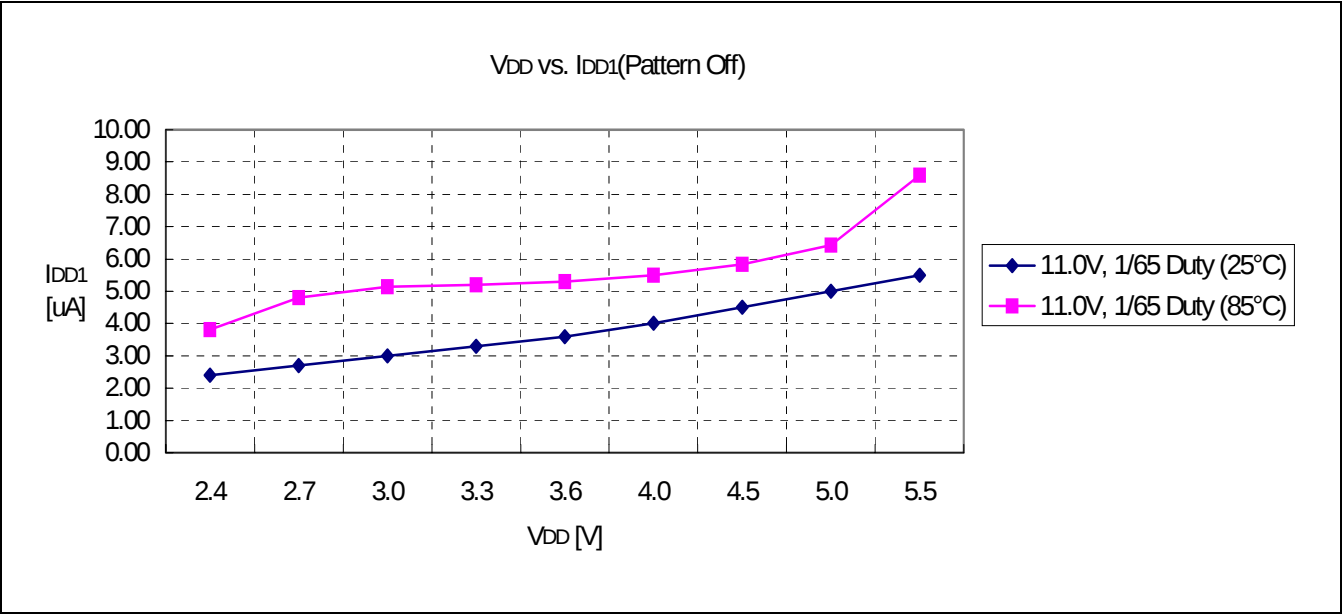


Figure 35. Display Pattern is OFF

IDD2 vs. VDD

\* Test Condition: Temperature: 25°C & 85°C, 1/65 duty, Quad Boosting, RR = 6, EV = 32

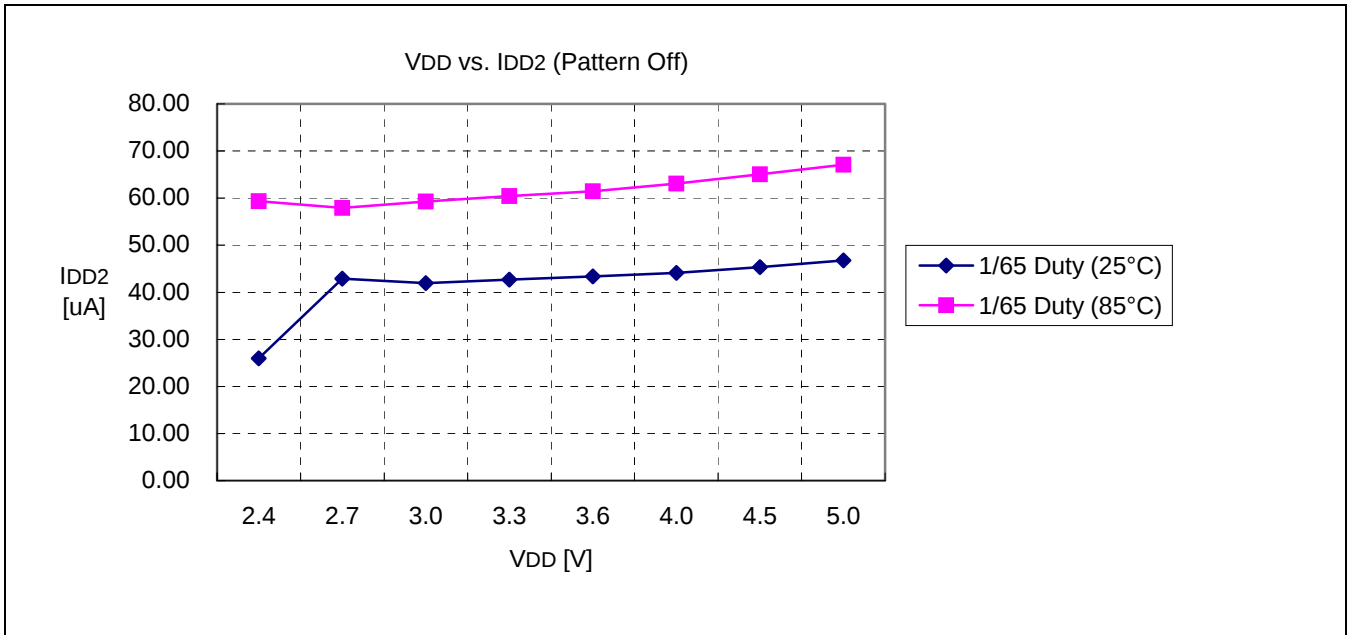


Figure 36. Display Pattern is OFF

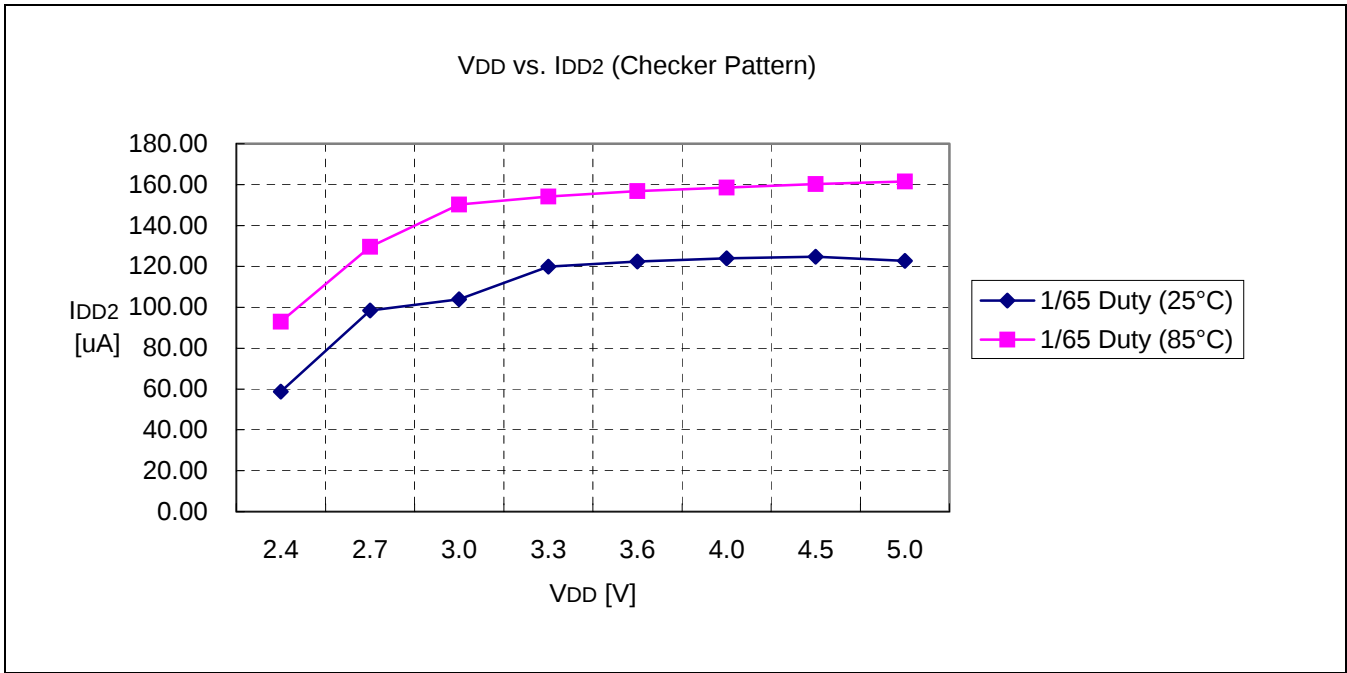


Figure 37. Display Pattern is Checker

## AC CHARACTERISTICS

## Read / Write Characteristics (8080-series MPU)

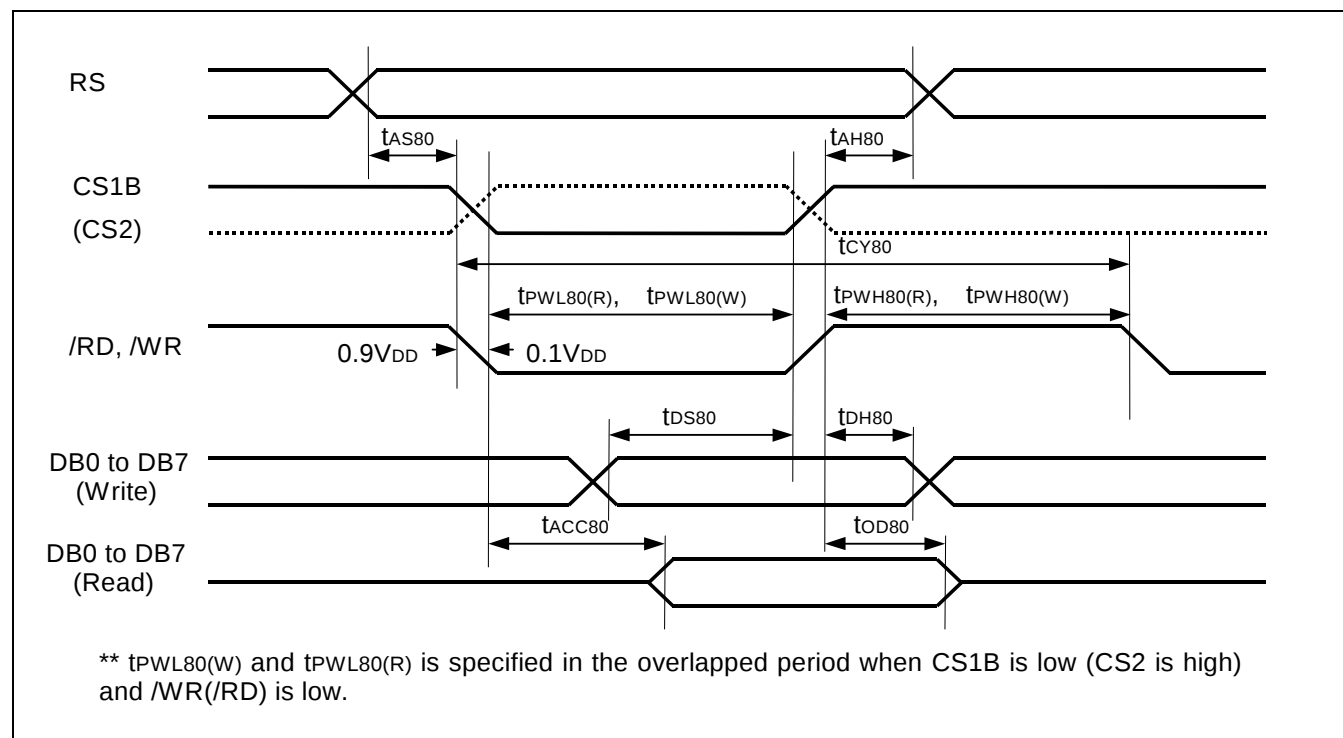


Figure 38. Read / Write Characteristics (8080-series MPU)

(V<sub>DD</sub> = 2.4 to 3.6V, T<sub>a</sub> = -40 to +85°C)

| Item                    | Signal           | Symbol   | Min.       | Typ. | Max. | Unit | Remark      |
|-------------------------|------------------|----------|------------|------|------|------|-------------|
| Address setup time      | RS               | tAS80    | 13         | -    | -    | ns   |             |
| Address hold time       |                  | tAH80    | 17         | -    | -    | ns   |             |
| System cycle time       | /WR, /RD         | tCY80    | 400        | -    | -    | ns   |             |
| Enable Pulse Low width  | Read             | /WR, /RD | tPWL80 (R) | 125  | -    | -    | ns          |
|                         | Write            |          | tPWL80 (W) | 55   | -    | -    | ns          |
| Enable Pulse High width | Read             | /WR, /RD | tPWH80 (R) | 245  | -    | -    | ns          |
|                         | Write            |          | tPWH80 (W) | 315  | -    | -    | ns          |
| Data setup time         | DB7<br>To<br>DB0 | tDS80    | 35         | -    | -    | ns   |             |
| Data hold time          |                  | tDH80    | 13         | -    | -    | ns   |             |
| Read access time        |                  | tACC80   | -          | -    | 125  | ns   | CL = 100 pF |
| Output disable time     |                  | tOD80    | 10         | -    | 90   | ns   |             |

(V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -40 to +85°C)

| Item                    | Signal           | Symbol   | Min.       | Typ. | Max. | Unit | Remark      |
|-------------------------|------------------|----------|------------|------|------|------|-------------|
| Address setup time      | RS               | tAS80    | 10         | -    | -    | ns   |             |
| Address hold time       |                  | tAH80    | 10         | -    | -    | ns   |             |
| System cycle time       | /WR, /RD         | tCY80    | 160        | -    | -    | ns   |             |
| Enable Pulse Low width  | Read             | /WR, /RD | tPWL80 (R) | 65   | -    | -    | ns          |
|                         | Write            |          | tPWL80 (W) | 25   | -    | -    | ns          |
| Enable Pulse High width | Read             | /WR, /RD | tPWH80 (R) | 65   | -    | -    | ns          |
|                         | Write            |          | tPWH80 (W) | 105  | -    | -    | ns          |
| Data setup time         | DB7<br>To<br>DB0 | tDS80    | 18         | -    | -    | ns   |             |
| Data hold time          |                  | tDH80    | 10         | -    | -    | ns   |             |
| Read access time        |                  | tACC80   | -          | -    | 65   | ns   | CL = 100 pF |
| Output disable time     |                  | tOD80    | 10         | -    | 45   | ns   |             |

Note The input signal rising time and falling time (tr, tf) is specified at 15ns or less.  
 Or (tr + tf) < (tCY80 – tPWL80 (W) – tPWH80 (W)) for write, (tr + tf) < (tCY80 – tPWL80 (R) – tPWH80 (R)) for read

## Read / Write Characteristics (6800-series Microprocessor)

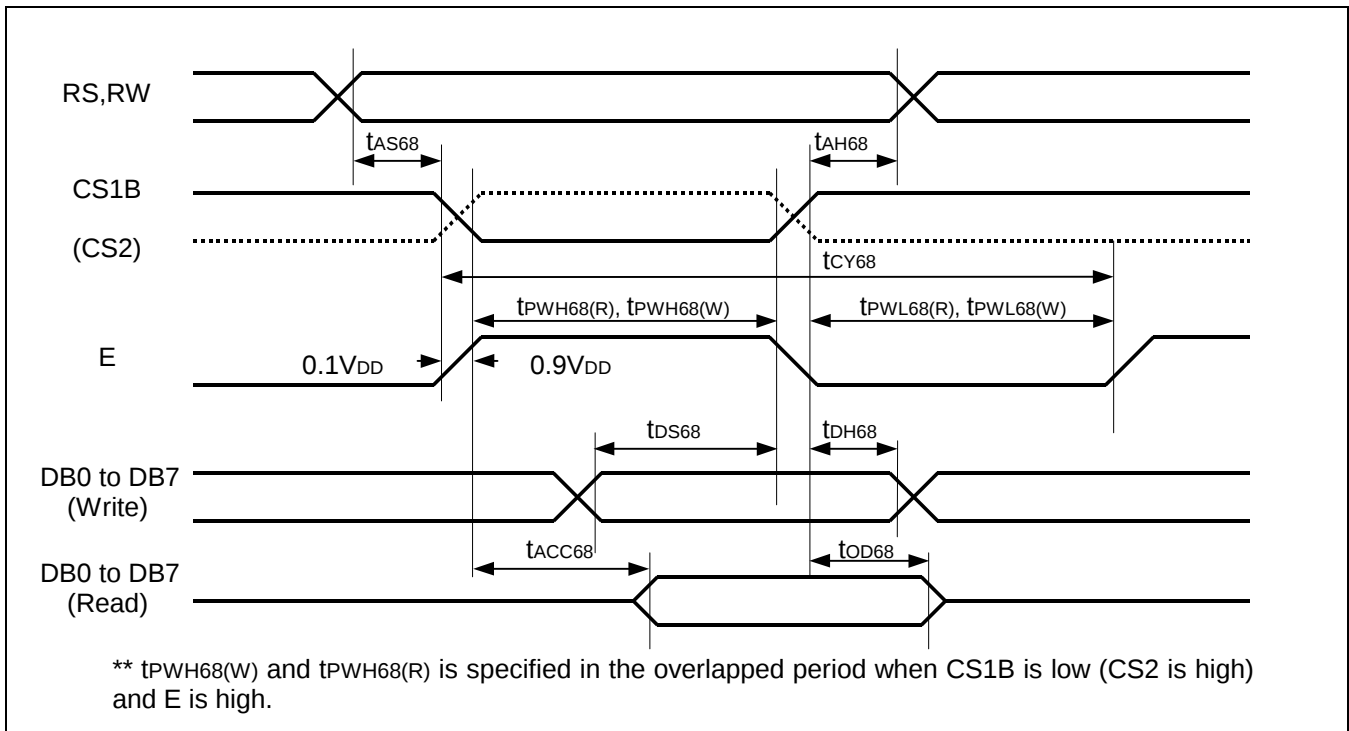


Figure 39. Read / Write Characteristics (6800-series Microprocessor)

(V<sub>DD</sub> = 2.4 to 3.6V, T<sub>a</sub> = -40 to +85°C)

| Item                                    | Signal           | Symbol         | Min.       | Typ. | Max. | Unit | Remark      |
|-----------------------------------------|------------------|----------------|------------|------|------|------|-------------|
| Address setup time<br>Address hold time | RS,RW            | tAS68<br>tAH68 | 13<br>17   | -    | -    | ns   |             |
| System cycle time                       | E                | tCY68          | 400        | -    | -    | ns   |             |
| Enable Pulse<br>Low Width               | Read             | E              | tPWL68 (R) | 125  | -    | -    | ns          |
|                                         | Write            |                | tPWL68 (W) | 55   | -    | -    |             |
| Enable Pulse<br>High Width              | Read             | E              | tPWH68 (R) | 245  | -    | -    | ns          |
|                                         | Write            |                | tPWH68 (W) | 315  | -    | -    |             |
| Data setup time<br>Data hold time       | DB7<br>To<br>DB0 | tDS68<br>tDH68 | 35<br>13   | -    | -    | ns   |             |
| Access time                             |                  | tACC68         | -          | -    | 125  | ns   | CL = 100 pF |
| Output disable time                     |                  | tOD68          | 10         | -    | 90   | ns   |             |

(V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -40 to +85°C)

| Item                                    | Signal           | Symbol         | Min.       | Typ. | Max. | Unit | Remark      |
|-----------------------------------------|------------------|----------------|------------|------|------|------|-------------|
| Address setup time<br>Address hold time | RS,RW            | tAS68<br>tAH68 | 10<br>10   | -    | -    | ns   |             |
| System cycle time                       | E                | tCY68          | 160        | -    | -    | ns   |             |
| Enable Pulse<br>Low Width               | Read             | E              | tPWL68 (R) | 65   | -    | -    | ns          |
|                                         | Write            |                | tPWL68 (W) | 25   | -    | -    |             |
| Enable Pulse<br>High Width              | Read             | E              | tPWH68 (R) | 65   | -    | -    | ns          |
|                                         | Write            |                | tPWH68 (W) | 105  | -    | -    |             |
| Data setup time<br>Data hold time       | DB7<br>To<br>DB0 | tDS68<br>tDH68 | 18<br>10   | -    | -    | ns   |             |
| Access time                             |                  | tACC68         | -          | -    | 65   | ns   | CL = 100 pF |
| Output disable time                     |                  | tOD68          | 10         | -    | 45   | ns   |             |

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less.

Or (tr + tf) &lt; (tCY68 – tPWL68 (W) – tPWH68 (W) ) for write, (tr + tf) &lt; (tCY68 – tPWL68 (R) – tPWH68 (R) ) for read.

## Serial Interface Characteristics

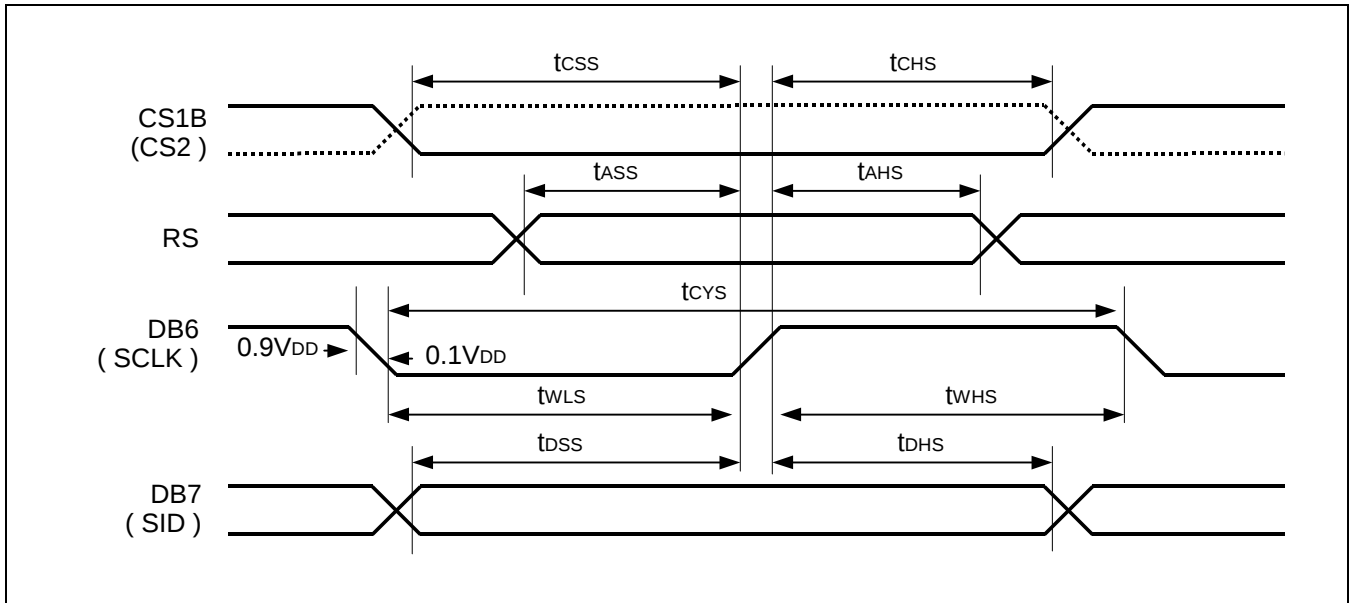


Figure 40. Serial Interface Characteristics

(V<sub>DD</sub> = 2.4 to 3.6V, T<sub>a</sub> = -40 to +85°C)

| Item                  | Signal     | Symbol           | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|------------|------------------|------|------|------|------|--------|
| Serial clock cycle    | DB6 (SCLK) | t <sub>CYS</sub> | 450  | -    | -    |      |        |
| SCLK high pulse width | DB6 (SCLK) | t <sub>WHS</sub> | 180  | -    | -    | ns   |        |
| SCLK low pulse width  | DB6 (SCLK) | t <sub>WLS</sub> | 135  | -    | -    |      |        |
| Address setup time    | RS         | t <sub>ASS</sub> | 90   | -    | -    | ns   |        |
| Address hold time     | RS         | t <sub>AHS</sub> | 360  | -    | -    |      |        |
| Data setup time       | DB7 (SID)  | t <sub>DSS</sub> | 90   | -    | -    | ns   |        |
| Data hold time        | DB7 (SID)  | t <sub>DHS</sub> | 90   | -    | -    |      |        |
| CS1B setup time       | CS1B       | t <sub>CSS</sub> | 55   | -    | -    | ns   |        |
| CS1B hold time        | CS1B       | t <sub>CHS</sub> | 180  | -    | -    |      |        |

(V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -40 to +85°C)

| Item                  | Signal     | Symbol           | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|------------|------------------|------|------|------|------|--------|
| Serial clock cycle    | DB6 (SCLK) | t <sub>CYS</sub> | 225  | -    | -    |      |        |
| SCLK high pulse width | DB6 (SCLK) | t <sub>WHS</sub> | 90   | -    | -    | ns   |        |
| SCLK low pulse width  | DB6 (SCLK) | t <sub>WLS</sub> | 70   | -    | -    |      |        |
| Address setup time    | RS         | t <sub>ASS</sub> | 45   | -    | -    | ns   |        |
| Address hold time     | RS         | t <sub>AHS</sub> | 180  | -    | -    |      |        |
| Data setup time       | DB7 (SID)  | t <sub>DSS</sub> | 45   | -    | -    | ns   |        |
| Data hold time        | DB7 (SID)  | t <sub>DHS</sub> | 45   | -    | -    |      |        |
| CS1B setup time       | CS1B       | t <sub>CSS</sub> | 25   | -    | -    | ns   |        |
| CS1B hold time        | CS1B       | t <sub>CHS</sub> | 90   | -    | -    |      |        |

## Reset Input Timing

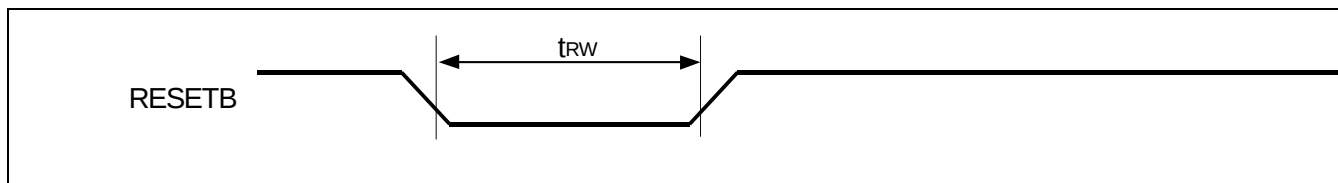


Figure 41. Reset Input Timing

(V<sub>DD</sub> = 2.4 to 3.6V, T<sub>a</sub> = -40 to +85°C)

| Item                  | Signal | Symbol   | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|--------|----------|------|------|------|------|--------|
| Reset low pulse width | RESETB | $t_{RW}$ | 900  | -    | -    | ns   |        |

(V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -40 to +85°C)

| Item                  | Signal | Symbol   | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|--------|----------|------|------|------|------|--------|
| Reset low pulse width | RESETB | $t_{RW}$ | 450  | -    | -    | ns   |        |

## REFERENCE APPLICATIONS

### MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", MI = "H")

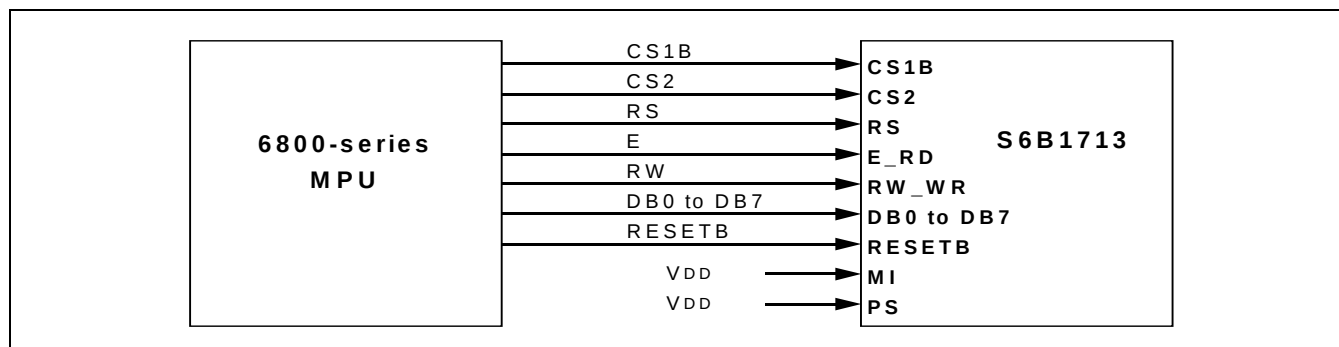


Figure 42. Interfacing with 6800-series (PS = "H", MI = "H")

In Case of Interfacing with 8080-series (PS = "H", MI = "L")

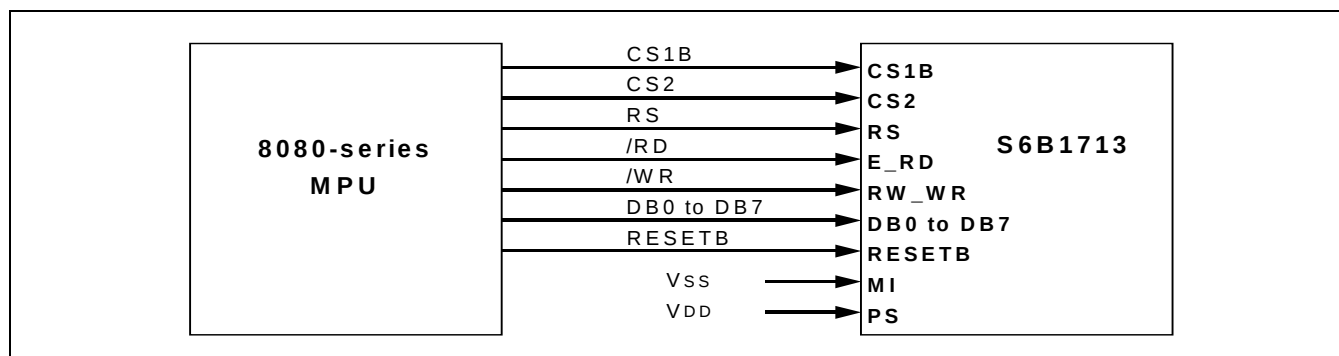


Figure 43. Interfacing with 8080-series (PS = "H", MI = "L")

In Case of Serial Interface (PS = "L", MI = "H/L")

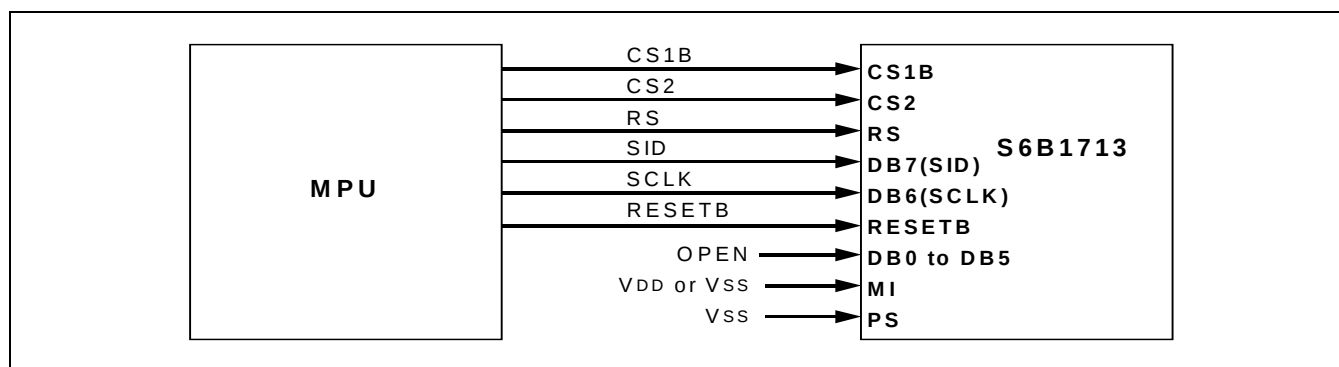


Figure 44. Serial Interface (PS = "L", MI = "H/L")

CONNECTIONS BETWEEN S6B1713 AND LCD PANEL

Single Chip Configuration (1/65 Duty Configurations)

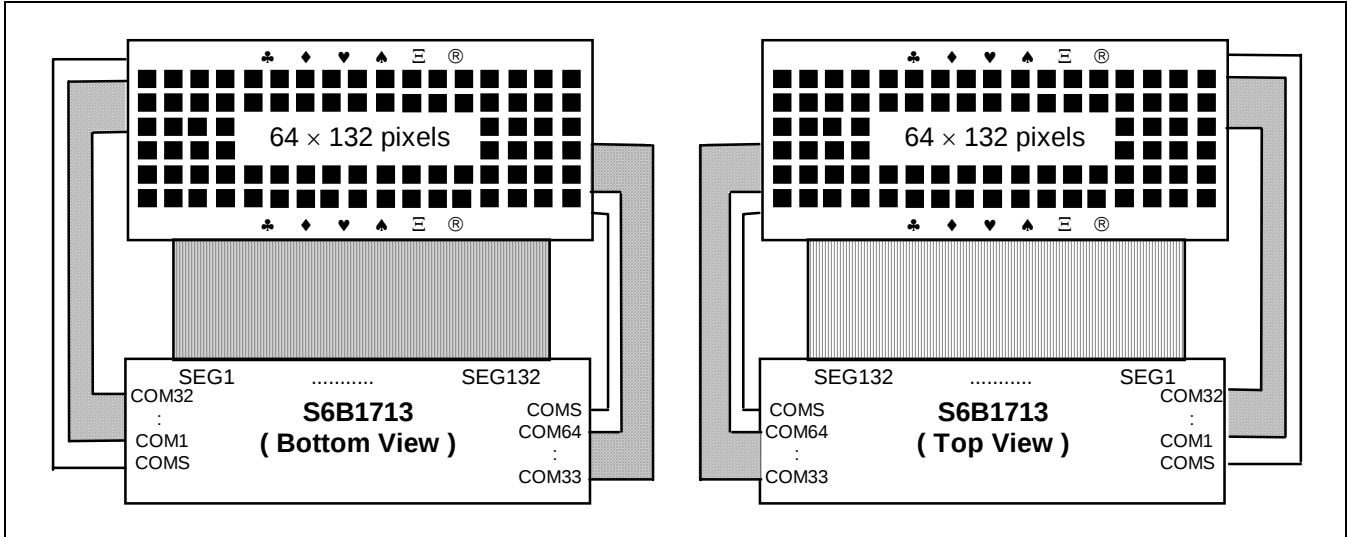


Figure 45. SHL = 0, ADC = 0

Figure 46. SHL = 0, ADC = 1

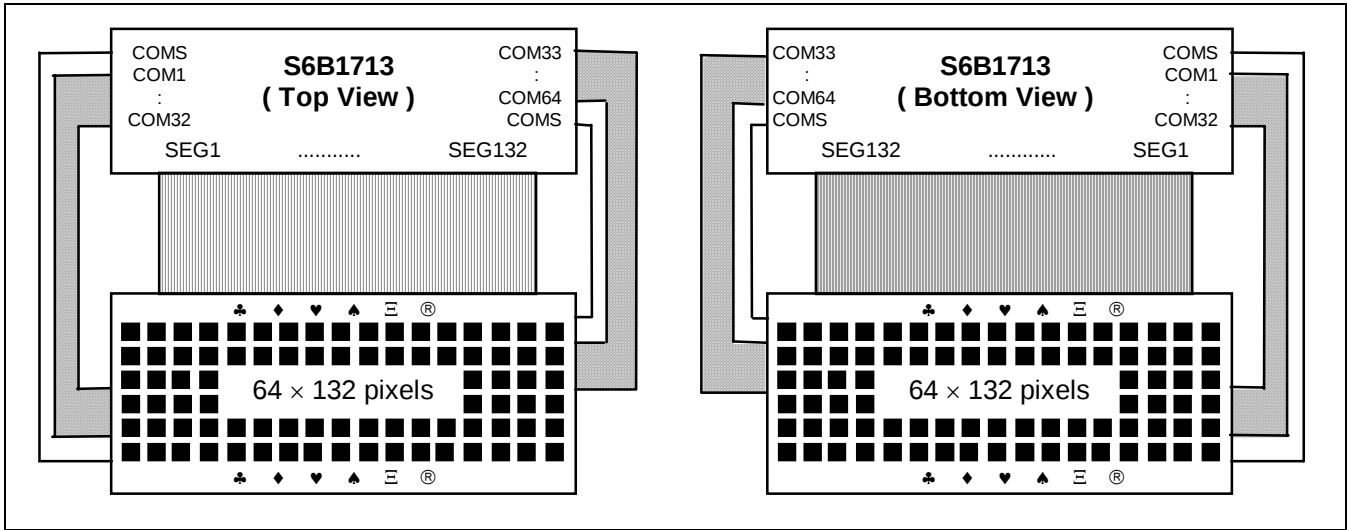


Figure 47. SHL = 1, ADC = 0

Figure 48. SHL = 1, ADC = 1

Single Chip Configuration (1/49 Duty Configurations)

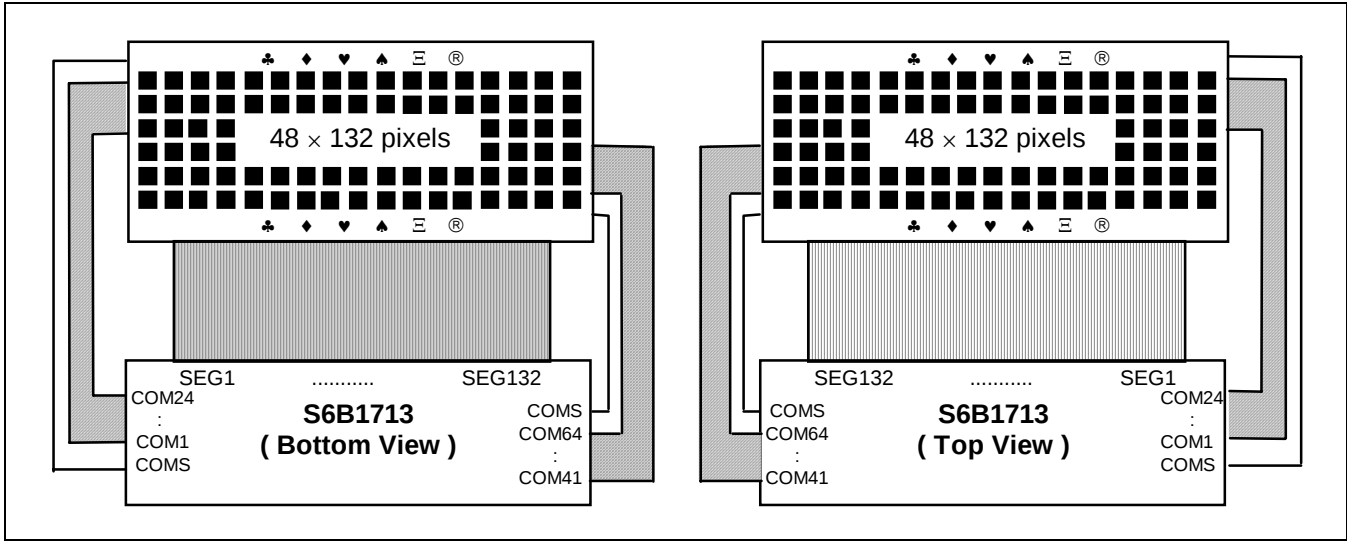


Figure 49. SHL = 0, ADC = 0

Figure 50. SHL = 0, ADC = 1

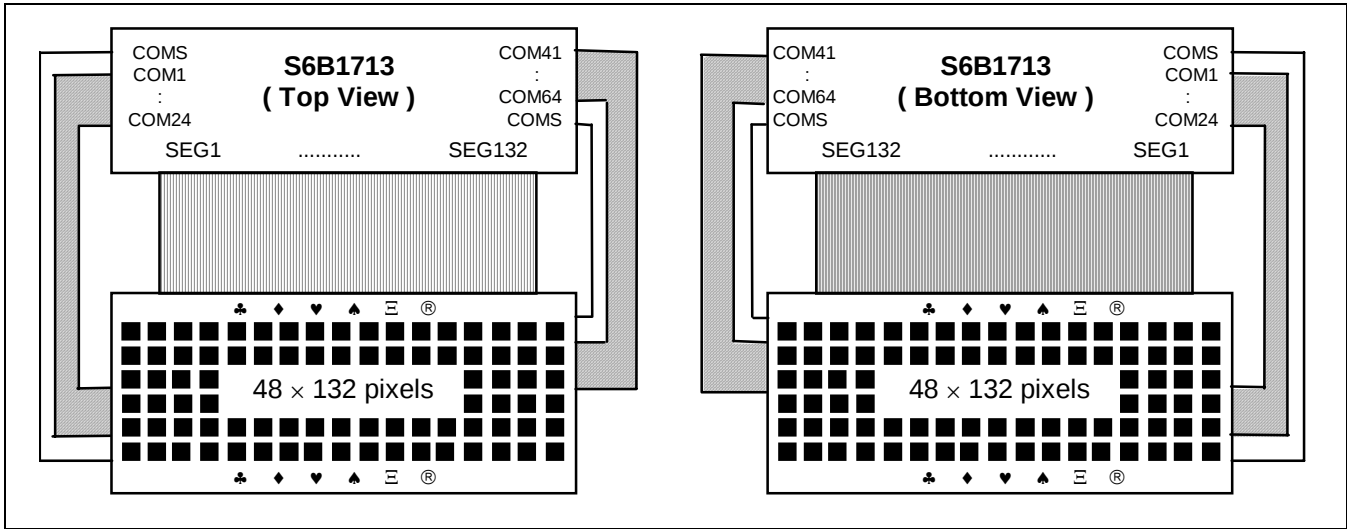


Figure 51. SHL = 1, ADC = 0

Figure 52. SHL = 1, ADC = 1

Single Chip Configuration (1/33 Duty Configurations)

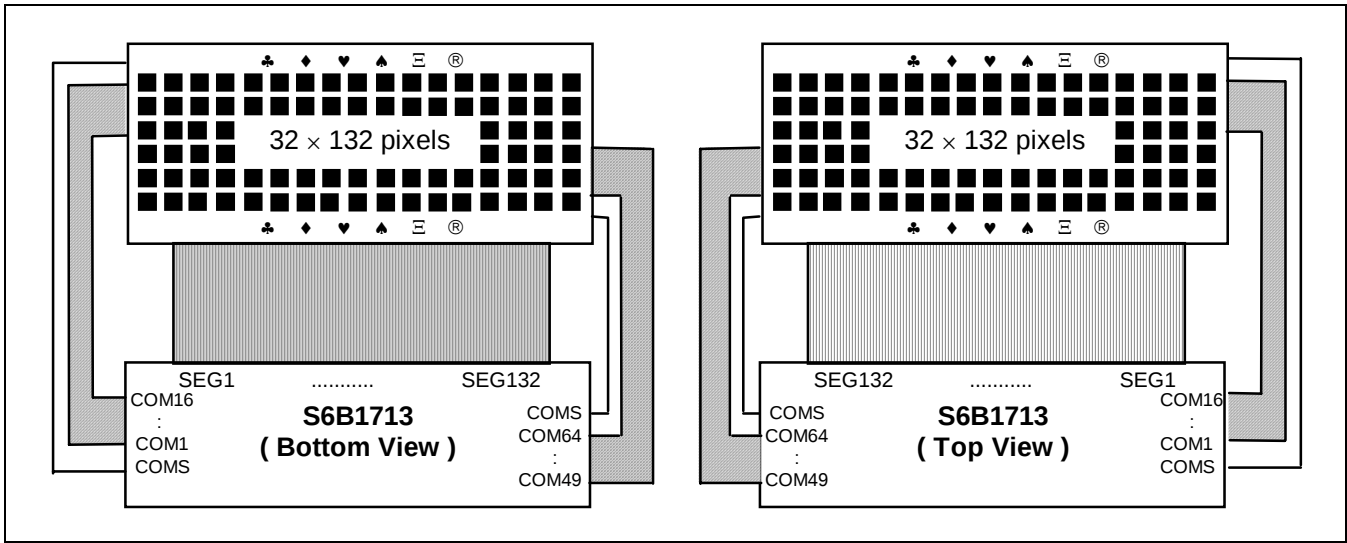


Figure 53. SHL = 0, ADC = 0

Figure 54. SHL = 0, ADC = 1

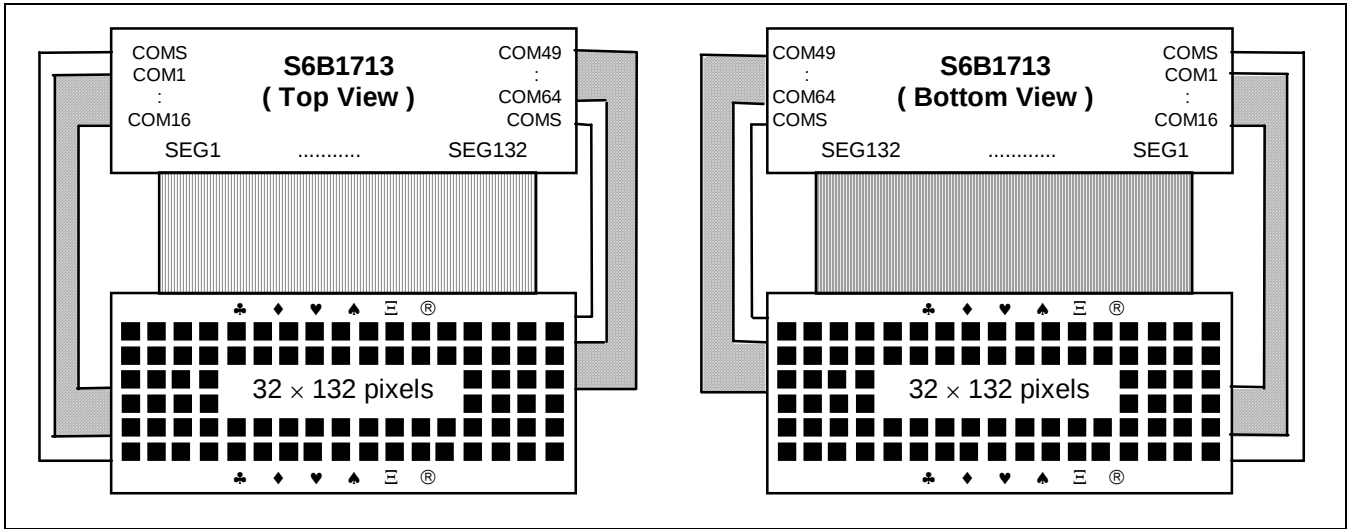


Figure 55. SHL = 1, ADC = 0

Figure 56. SHL = 1, ADC = 1

TCP PIN LAYOUT (SAMPLE)

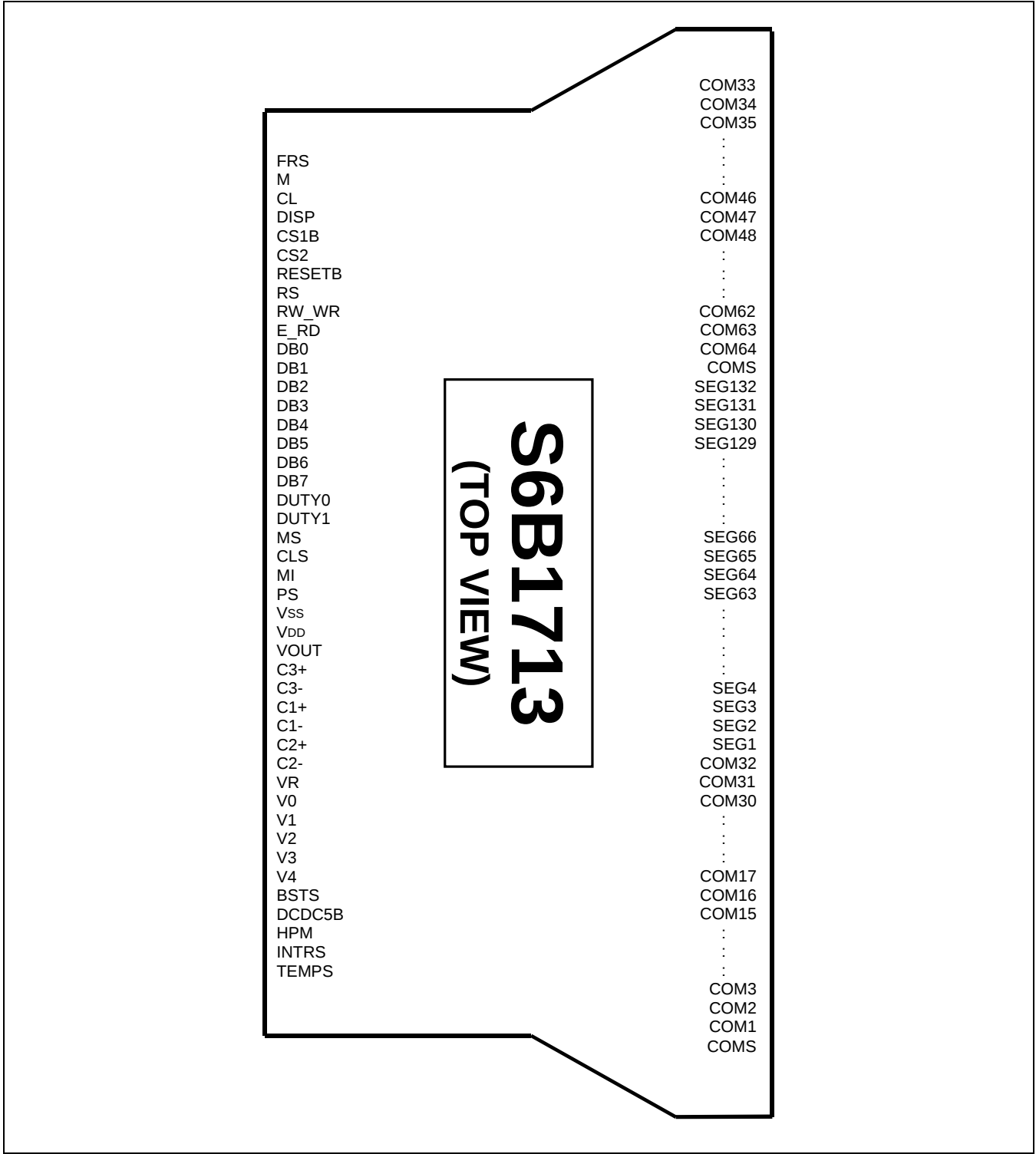


Figure 57. TCP Pin Layout

| S6B1713 Specification Revision History |                                                                                                                                                      |           |
|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| Version                                | Content                                                                                                                                              | Date      |
| 2.0                                    | Neglect the more past version than version 2.0                                                                                                       | Nov.1998  |
| 2.1                                    | fosc = 16kHz (Typ.) → 22kHz (Typ.): For removing flicker phenomenon<br>Temperature coefficient (when TEMPS = L): -0.0%/°C → -0.05%/°C                | Nov.1998  |
| 3.0                                    | Modified some syntax errors<br>Voltage regulator reference voltage [VREF]: TBD → 2.0<br>Modified voltage regulator block of "Functional Description" | Nov.1998  |
| 3.1                                    | VLCD absolute maximum rating: 15.0V → 17.0V<br>Power consumption: 100μA → 80μA                                                                       |           |
| 3.2                                    | Oscillator frequency (1): 19 (Min.) → 17 (Min.), 25 (Max.) → 27 (Max.)<br>Oscillator frequency (2): 22 (Min.) → 20 (Min.), 28 (Max.) → 30 (Max.)     |           |
| 3.3                                    | Modified Y-axis values of "Pad Center Coordinates"<br>Modified the contents of "Referential Instruction Setup Flow"                                  |           |
| 3.4                                    | Word-processor version change                                                                                                                        | Apr.1999  |
| 3.5                                    | Modified error: pad No.113 (COMS) Y Coordinate: -1210 → -1140 (after)                                                                                | Oct.1999  |
| 4.0                                    | Change VDD Range : 2.4V to 5.5V → 2.4V to 3.6V                                                                                                       | Jan.2000  |
| 4.1                                    | Added detail information for several items                                                                                                           | Mar.2001  |
| 4.2                                    | Change VDD Range : 2.4V to 3.6V → 2.4V to 5.5V                                                                                                       | Mar.2002  |
| 4.3                                    | Removed the master-slave function                                                                                                                    | Mar. 2004 |